General Description

The CT560X is a family of a high performance Primary Side Regulation (PSR) power switch with high precision CV/CC control ideal for charger applications. The IC can also support Quasi-Resonant (QR) Buck constant current topology for LED lighting if SEL pin is short to GND.

In CV mode, The CT560X adopts Multi Mode Control which uses the hybrid of AM (Amplitude Modulation) mode and (Frequency Modulation) FM mode to improve system efficiency and reliability. In CC mode, the IC uses PFM control with line and load CC compensation. The IC can achieve audio noise free operation and optimized dynamic response. The built-in Cable Drop Compensation (CDC) function can provide excellent CV performance.

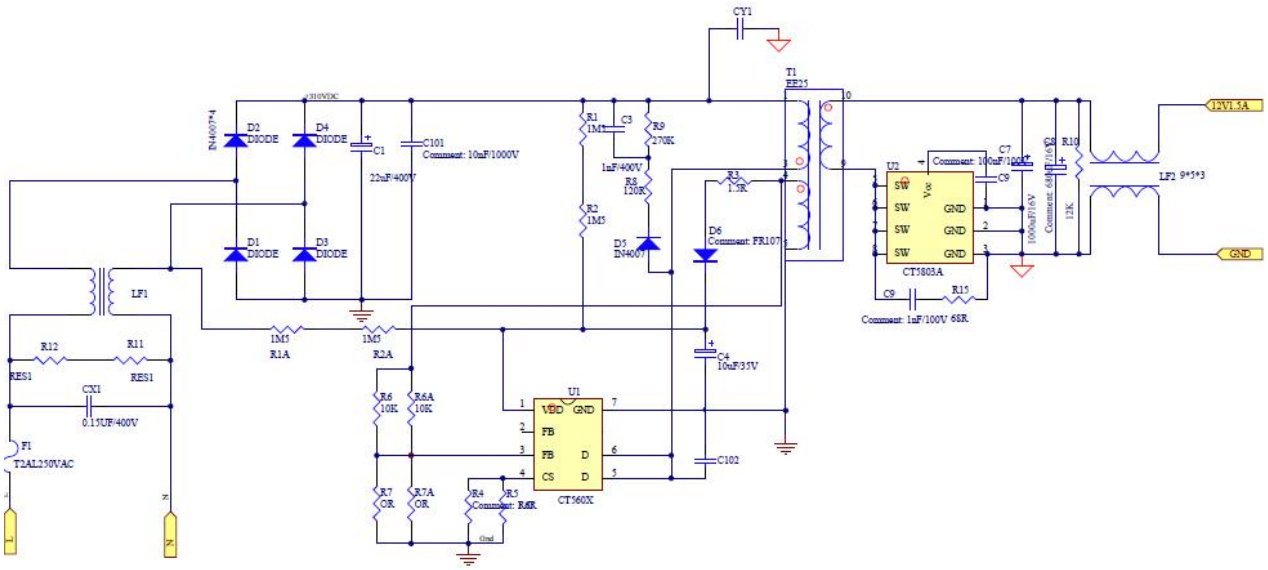
The CT560X integrates functions and protections of Under Voltage Lockout (UVLO), VCC over Voltage Protection (VCC OVP), Cycle-by-cycle Current Limiting (OCP), Short Load Protection (SLP), and VCC Clamping.

The CT5603S is available in DIP-7 package, and CT5604D/CT5605D are available in DIP-7 package.

Features

- Integrated with 650V MOSFET
- Multi Mode PSR Control
- Audio Noise Free Operation for PSR
- Optimized Dynamic Response for PSR
- Low Standby Power <70mW
- ±4% CC and CV Regulation
- Programmable Cable Drop Compensation (CDC) in PSR CV Mode
- Built-in AC Line & Load CC Compensation
- Build in Protections:
  - Short Load Protection (SLP)
  - On-Chip Thermal Shutdown (OTP)
  - Cycle-by-Cycle Current Limiting
  - Leading Edge Blanking (LEB)
  - Pin Floating Protection
  - VCC UVLO, OVP & Clamp

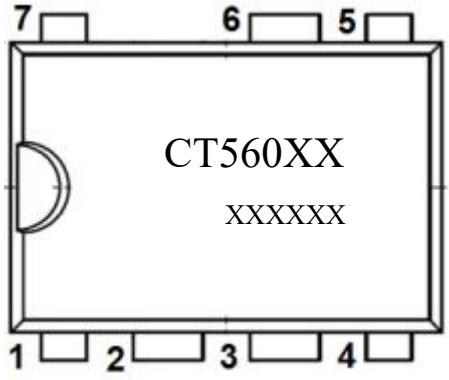
Typical Application



Ordering Information

Part Number	Package	Package Method	Marking
CT5603S（SOP-7）	SOP-7	Tape 4,000pcs/Roll	CT5603S XXXXXX
CT5604D（DIP-7）	DIP-7	Tube 50pcs/Tube	CT5604D XXXXXX
CT5605D（DIP-7）	DIP-7	Tube 50pcs/Tube	CT5605D XXXXXX

Pin Assignment



Pin Description

Pin	Pin Name	Description
VCC	1	IC Supply Voltage input
FB	2/3	System feedback pin which regulates both the output voltage in CV mode and output current in CC mode based on the flyback voltage of the auxiliary winding
CS	4	Current sense input
D	5/6	The Power MOSFET Drain
GND	7	IC Ground

Recommended Operation Conditions

Part Number	230VAC ± 15%(2)	85-265VAC
	Adapter(2)	Adapter(2)
CT5603S	12W	10W
CT5604D	18W	15W
CT5605D	24W	18W

Note 1. The Max. output power is limited by junction temperature

Note 2. Typical continuous power in a non-ventilated enclosed adapter with sufficient drain pattern as a heat sink at 50℃ ambient.

Absolute Maximum Ratings

Parameter	Symbol	Parameter Range	Unit
DRAIN pin Voltage(D)	V_{DRAIN}	-0.3~650	V
Supply Voltage（VCC）	V_{VCC}	34.5	V
FB pin Voltage （FB）	V_{FB}	-0.7~7	V
CS pin voltage （CS）	V_{CS},V_E	-0.3~7	V
OUT pin output current	I_{OUT}	Internal limited	A
Maximum Power Dissipation (Ta=25°C)	P_{tot}	0.45@ SOP-7	W
		0.90@ DIP-7	
Thermal Resistance Junction-ambient	Rthj-a	145@ SOP-7	°C/W
		80@ DIP-7	
Operating Junction Temperature	T_J	-40～150	°C
Storage Temperature Range	T_{STG}	-55～150	°C
V_{ESD_HBM}	Human Body Model	2,000	V
V_{ESD_MM}	Machine Model	200	V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability。

Recommended Operation Conditions

Parameter	Value	Unit
Supply Voltage, V_{CC}	11 to 27	V
Operating Ambient Temperature	-40 to 85	°C
Maximum Switching Frequency @ Full Loading	70	kHz
Minimum Switching Frequency @ Full Loading	35	kHz

Note2. The device is not guaranteed to function outside its operating conditions.

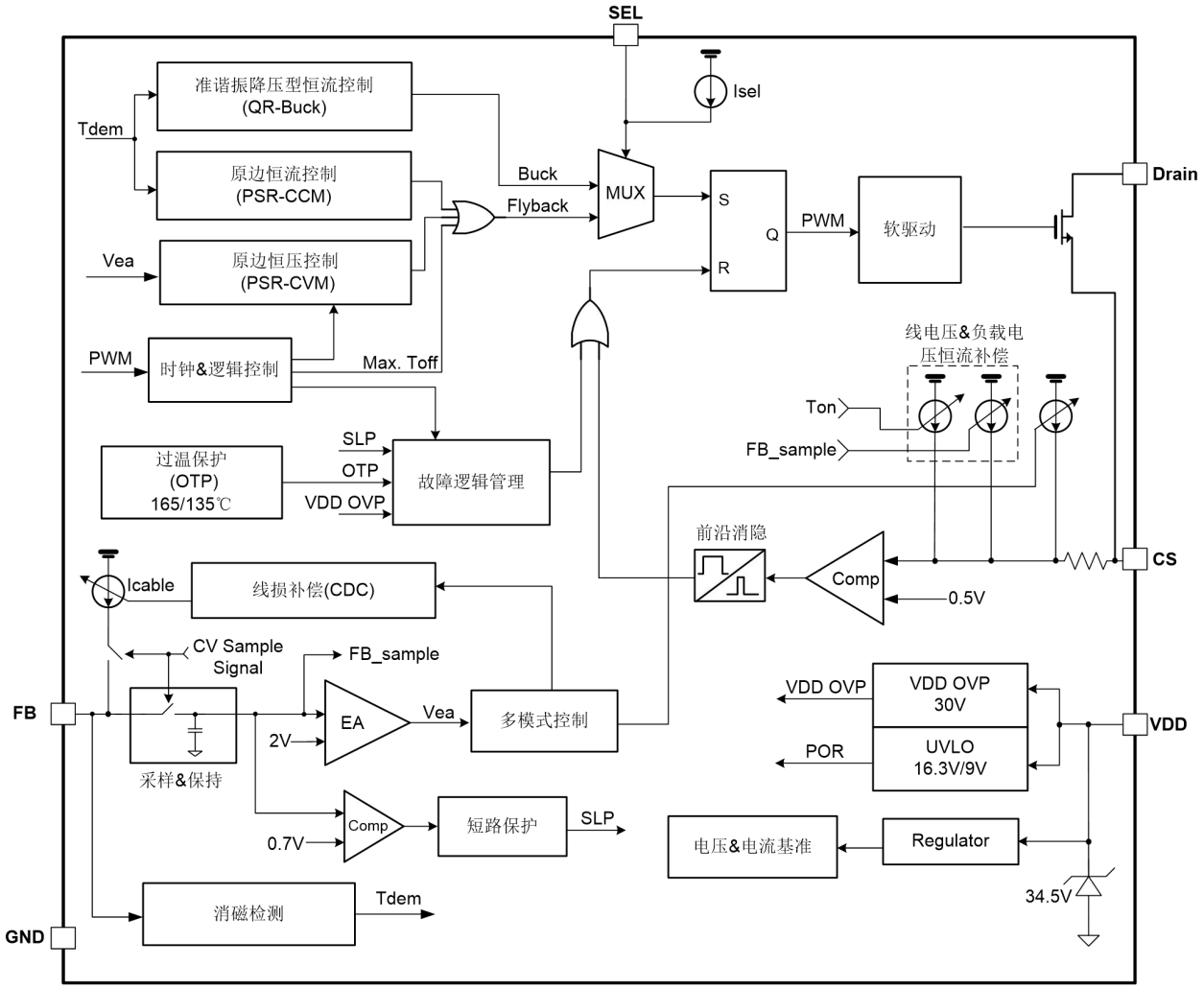
Electronic Characteristics

T_C=25°C,V_{CC} = 18V,unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Section(V_{CC} Pin)						
I_{VCC_st}	Start-up current into V_{CC} pin			2	15	uA
I_{VCC_Op}	Operation Current	V_{FB}=1.1V, V_{CC}=18V	0.3	0.7	0.9	mA
$I_{VCC\_standby}$	Standby Current			0.5	1	mA
V_{CC_ON}	V_{CC} Under Voltage Lockout Exit		15	16.3	17.5	V
V_{CC_OFF}	V_{CC} Under Voltage Lockout Enter		8	9	10	V
V_{CC_OVP}	V_{CC} OVP Threshold		28	30	32	V
V_{CC_Clamp}	V_{CC} Zener Clamp Voltage	I(V_{CC}) = 7 mA	32.5	34.5	36.5	V
Control Function Section (FB Pin)						
V_{FBREF}	Internal Error Amplifier (EA) Reference Input		1.97	2.0	2.03	V
V_{FB_SLP}	Short Load Protection (SLP) Threshold			0.7		V
T_{FB_Short}	Short Load Protection (SLP) Debounce Time			10		ms
V_{FB_DEM}	Demagnetization Comparator Threshold			25		mV
T_{off_min}	Minimum OFF time			2		us
T_{off_max}	Maximum OFF time		3.6	4	4.5	ms
I_{Cable_max}	Maximum Cable Drop Compensation(CDC) Current		48	53	58	uA
Current Sense Input Section (CS Pin)						
T_{LEB}	CS Input Leading Edge Blanking Time			500		ns
$V_{cs(max)}$	Current limiting threshold		490	500	510	mV
T_{D_OC}	Over Current Detection and Control Delay			100		ns
Power MOSFET Section (D Pin)						

BV_{dss}	MOSFET Drain-Source Breakdown Voltage		650	-		V
Rds(on)	Static Drain-Source On Resistance	CT5603S		2.5	2.8	Ω
		CT5604D		2.5	2.8	Ω
		CT5605D		1.8	2.0	Ω
On-Chip Thermal Shutdown						
T_Z	Intelligent Thermal Control Threshold	Output Power Shut Down	---	165	--	℃
T_{OTP}	OTP Threshold	Restart		135	--	℃

Functional Block Diagram



Applications Information

Functional Description

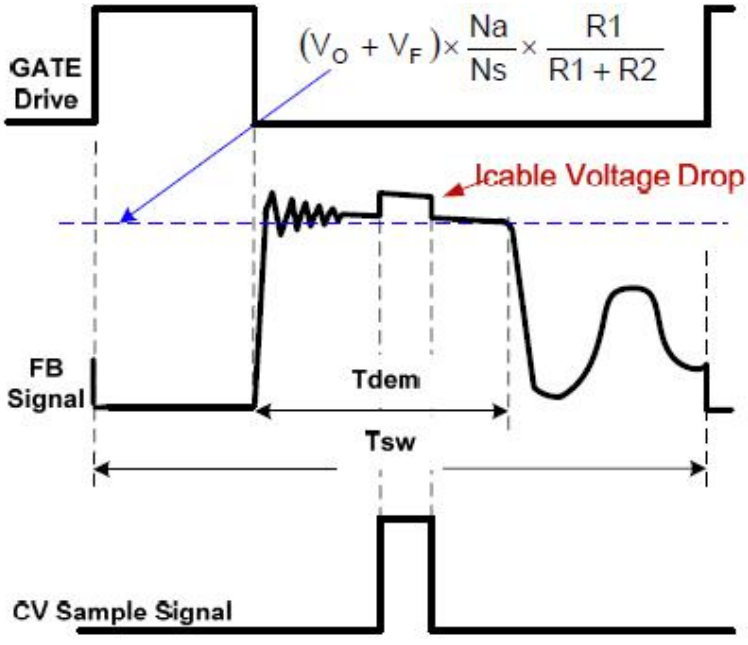
The CT560X is a family of multi-mode, highly integrated DCM (Discontinuous Conduction Mode) Primary Side Regulation (PSR) power switch. The built-in high precision CV/CC control with high level protection features makes it suitable for offline small power converter applications.

System Start-Up Operation

Before the IC starts to work, it consumes only startup current (typically 2uA) which allows a large value startup resistor to be used to minimize the power loss and the current flowing through the startup resistor charges the VCC hold-up capacitor from the high voltage DC bus. When VCC reaches UVLO turn-on voltage of 16.3V (typical), the CT560X begins switching and the IC operation current is increased to be 1mA (typical).
The hold-up capacitor continues to supply VCC before the auxiliary winding of the transformer takes the control of VCC voltage. Once CT560X enters very low frequency FM (Frequency Modulation) mode, the operating current is reduced to be 0.5mA typically, which helps to reduce the standby power loss.

Quasi Resonant PSR CV Modulation (QR-CVM)

In primary side control, the output voltage is sensed on the auxiliary winding during the transfer of transformer energy to the secondary. The below Fig. illustrates the CV sampling signal timing waveform in CT560X. As shown in the Fig., it is clear that there is a down slope representing a decreasing total rectifier VF and its voltage drop as the secondary current decreases to zero. To achieve an accurate representation of the secondary output voltage on the auxiliary winding, the CV sampling signal blocks the leakage inductance reset and ringing. When the CV sampling process is over, the internal sample/hold (S&H) circuit captures the error signal and amplifies it through the internal Error Amplifier (EA). The output of EA is sent to the PSR Constant Voltage Modulator (PSR-CVM) for CV control. The internal reference voltage for EA is trimmed to 2V with high accuracy.



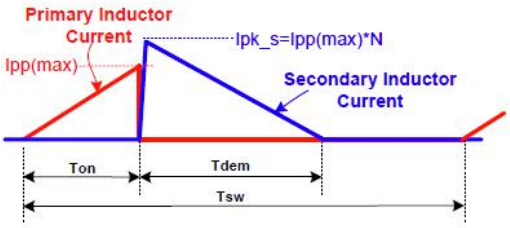
During the CV sampling process, an internal variable current source is flowing to FB pin for Cable Drop Compensation (CDC). Thus, there is a step at FB pin in the transformer demagnetization process, as shown in the Fig., the Fig. also illustrates the equation for

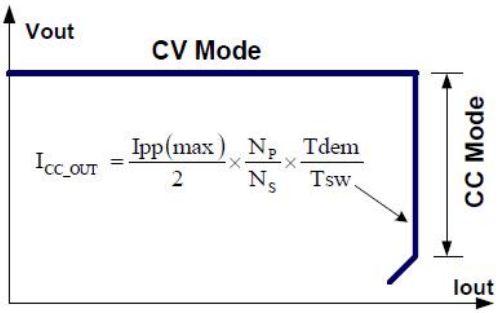
"demagnetization plateau", where Vo and VF is the output voltage and diode forward voltage; R1 and R2 is the resistor divider connected from the auxiliary winding to FB Pin, Ns and Na are secondary winding and auxiliary winding respectively.

When system enters over load condition, the output voltage falls down and the FB sampled voltage should be lower than 2V internal reference which makes system enter CC Mode automatically.

PSR Constant Current Modulation (PSR-CCM)

Timing information at the FB pin and current information at the CS pin allow accurate regulation of the secondary average current. The control law dictates that as power is increased in CV regulation and approaching CC regulation the primary peak current is at Ipp(max), as shown in the Fig. on the right.





Referring to the Fig. on the right, the primary peak current, transformer turns ratio, secondary demagnetization time (Tdem), and switching period (Tsw) determines the secondary average output current Iout. Ignoring leakage inductance effects, the equation for average output current is shown in the Fig. When the average output current Iout reaches the regulation reference in the PSR Constant Current Modulator (PSR-CCM) block, the IC operates in pulse frequency modulation (PFM) mode to control the output current at any output voltage at or below the voltage regulation target as long as the auxiliary winding can keep VCC above the UVLO turn-off threshold.

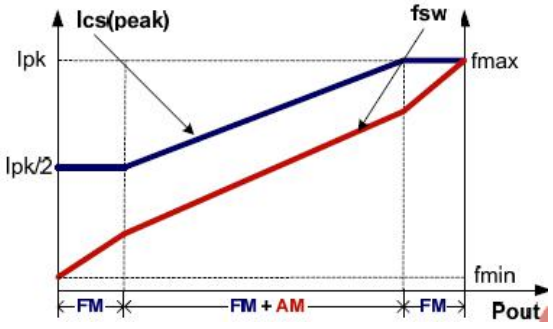
In CT560X, the ratio between Tdem and Tsw in CC mode is 1/2. Therefore, the average output current can be expressed as:

$$I_{CC\_OUT}(mA) \cong \frac{1}{4} \times N \times \frac{500mV}{Rcs(\Omega)}$$

Where,
N----The turn ratio of primary side winding to secondary side winding.
Rcs---The sensing resistor connected between the power MOSFET source to GND.

Multi Mode Control in CV Mode

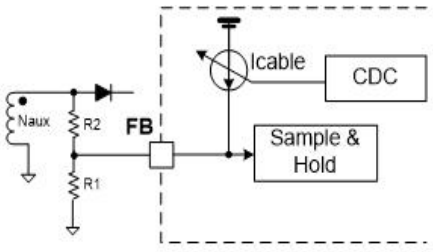
To meet the tight requirement of averaged system efficiency and no load power consumption, a hybrid of frequency modulation (FM) and amplitude modulation (AM) is adopted in CT560X which is shown in the Fig on the right. Around the full load, the system operates in FM mode. When normal to light load conditions, the IC operates in FM+AM mode to



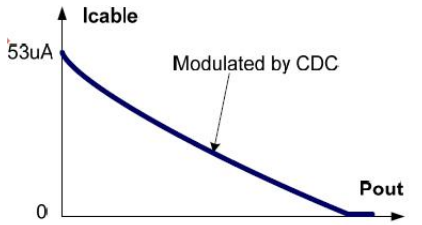
achieve excellent regulation and high efficiency. When the system is near zero loading, the IC operates in FM again for standby power reduction. In this way, the no-load consumption can be less than 70mW.

Programmable Cable Drop Compensation (CDC) in CV Mode

In smart phone charger application, the battery is always connected to the adapter with a cable wire which can cause several percentages of voltage drop on the actual battery voltage. In CT560X, an offset voltage is generated at FB pin by an internal current source (modulated by CDC block, as shown in the Fig. as below) flowing into the resistor divider.



The current is proportional to the switching period, thus, it is inversely proportional to the output power Pout. Therefore, the drop due the cable loss can be compensated. As the load decreases from full loading to zero loading, the offset voltage at FB pin will increase. By adjusting the resistance of R1 and R2 (as shown in the Fig.), the cable loss compensation can be programmed. The percentage of maximum compensation is given by



$$\frac{\Delta V(cable)}{Vout} \approx \frac{Icable\_max \times (R1//R2)}{V_{FB\_REF}} \times 100\%$$

For example, R1=3K Ω , R2=18K Ω , The percentage of maximum compensation is given by:

$$\frac{\Delta V(cable)}{Vout} = \frac{53uA \times (3K//18K)}{2V} \times 100\% = 8.1\%$$

Optimized Dynamic Response for PSR

In CT560X, the dynamic response performance is optimized to meet USB charge requirements.

Audio Noise Free Operation for PSR

As mentioned above, the multi-mode CV control with a hybrid of FM and AM provides frequency modulation. An internal current source flowing to CS pin realizes CS peak voltage modulation. In CT560X, the optimized combination of frequency modulation and CS peak voltage modulation algorithm can provide audio noise free operation from full loading to zero loading.

Short Load Protection (SLP)

In CT560X, the output is sampled on FB pin and then compared with a threshold of UVP (0.7V typically) after an internal blanking time (10ms typical). In CT560X, when sensed FB voltage is below 0.7V, the IC will enter into Short Load Protection (SLP) mode, in which the IC will enter into auto recovery protection mode.

VCC Over Voltage Protection (OVP) and Zener Clamp

When VCC voltage is higher than 30V (typical), the IC will stop switching. This will cause

VCC fall down to be lower than VCC_OFF (typical 9V) an then the system will restart up again. An internal 34.5V (typical) zener clamp is integrated to prevent the IC from damage.

On Chip Thermal Shutdown (OTP)

When the IC temperature is over 165 oC, the IC shuts down. Only when the IC temperature drops to 135 oC, IC will restart.

Pin Floating Protection

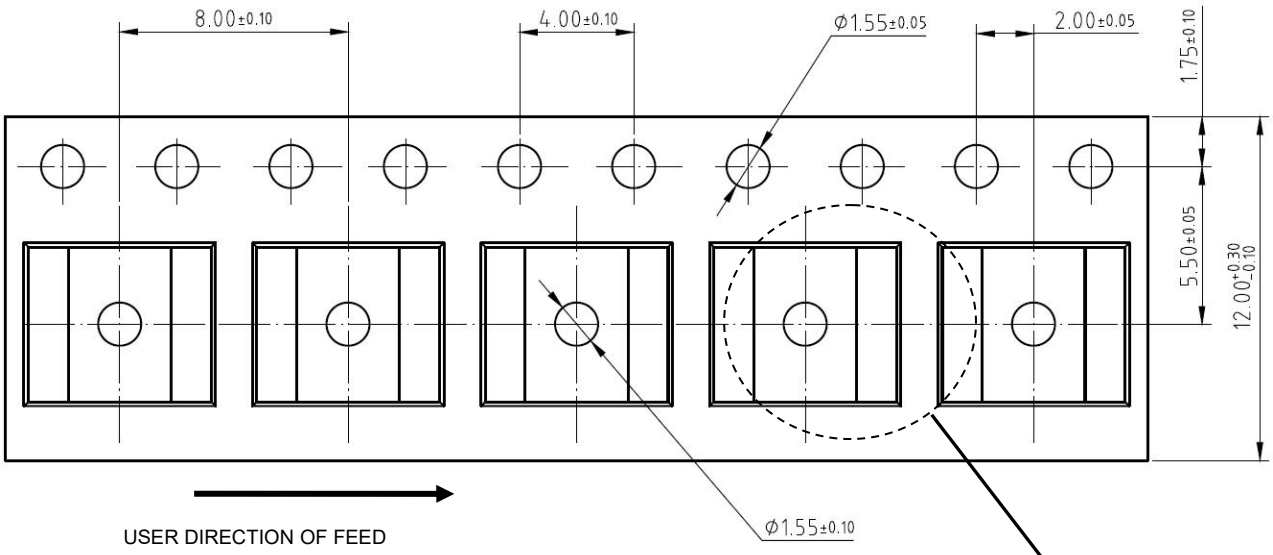
In CT560X, if pin floating situation occurs, the IC is designed to have no damage to system.

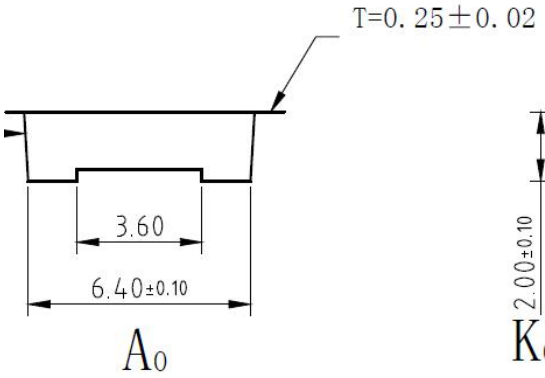
Soft Totem-Pole Gate Driver

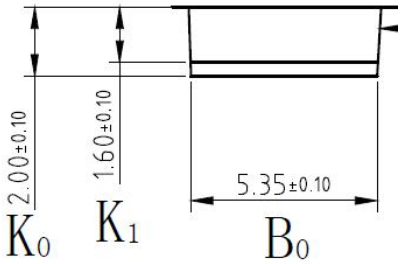
The CT560X has a soft totem-pole gate driver with optimized EMI performance. An internal 16Vclamp is added for power MOSFET gate protection when high VCC input.

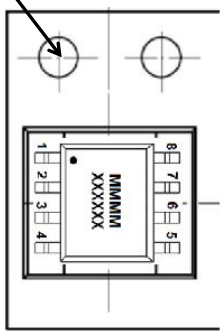
SOP-7/8 (13")TAPE AND REEL DATA

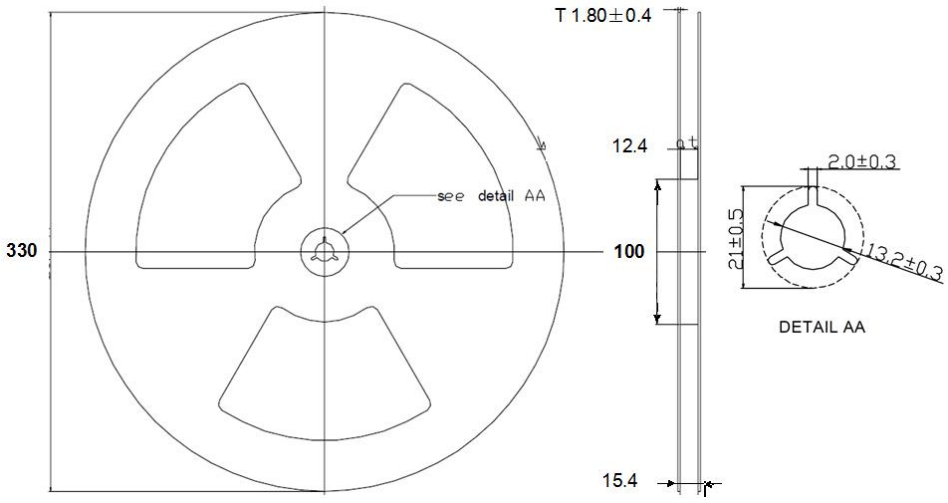
UNIT：mm









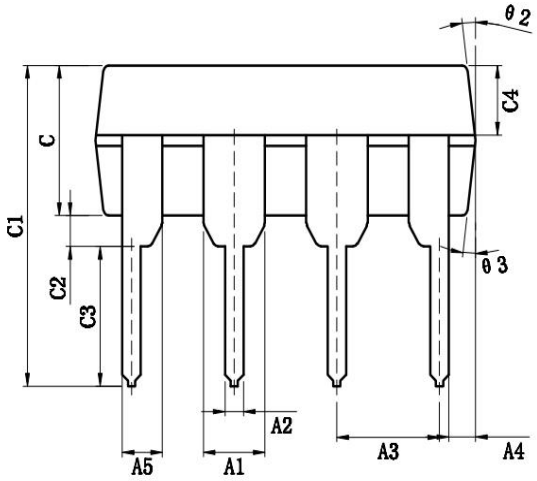


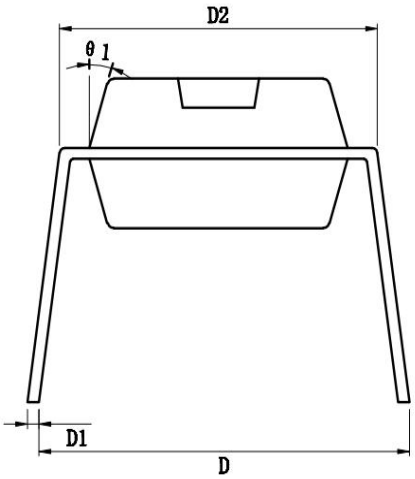
13" REEL

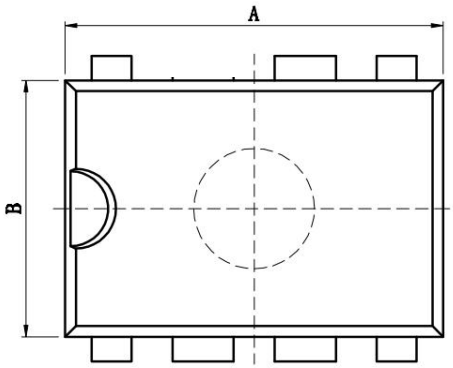
DIP-7 MECHANICAL DATA

UNIT：mm

SYMBOL	min	nomarl	max	SYMBOL	min	nomarl	max
A	9.00		9.20	C2		0.50TYP	
A1	1.474		1.574	C3	3.20		3.40
A2	0.41		0.51	C4	1.47		1.57
A3	2.44		2.64	D	8.20		8.80
A4		0.51TYP		D1	0.244		0.264
A5		0.99TYP		D2	7.62		7.87
B	6.10		6.30	Θ1		17°TYP4	
C	3.20		3.40	Θ2		10°TYP4	
C1	7.10		7.30	Θ3		8°TYP	







Revision history

Revision	Release data	Description
1.0	2015-12-1	Initial Version