General Description

CT5601 is a high performance current mode PWM controller for offline flyback converter applications. The CT5601 has built-in General Primary Side CC control, which simplifies isolated power supply design that requires CC regulation of the output.

In CT5601, PWM switching frequency with shuffling is fixed to 65 KHz and is trimmed to tight range. The CT5601 has built-in green and burst mode control for light and no load condition, which can achieve less than 75mW standby power for sub 30W applications.

The CT5601 integrates functions and protections of Under Voltage Lockout (UVLO), VCC over Voltage Protection (VCC OVP), Cycle-by-cycle Current Limiting (OCP), Short Circuit Protection (SCP), Over Load Protection (OLP), On-Chip Thermal Shutdown (OTP), Soft Start, VCC clamping and CS Pin Float Protection, etc.

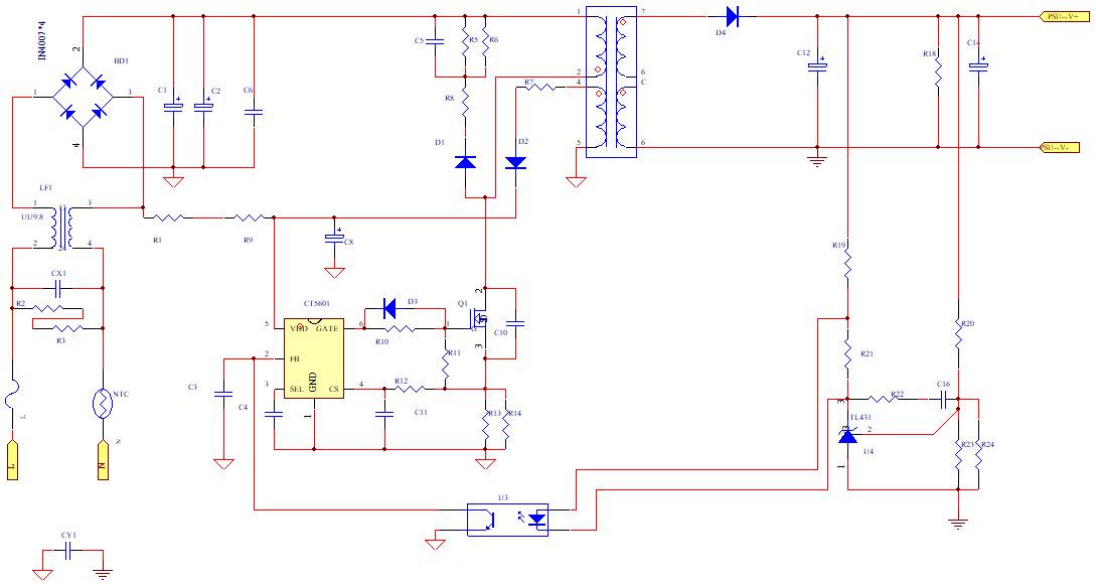
The CT5600 is available in SOT23-6 package.

Features

- Primary Side Constant-Current (CC) Control for DCM and CCM Operation
- ±5% CC Regulation; ±1% CV Regulation
- Less than 75mW Standby Power
- Fixed 65KHz Switching Frequency
- Green Mode and Burst Mode Control
- Very Low Startup and Operation Current
- Built-in Frequency Shuffling to Reduce EMI
- Built-in Current Mode Control with Internal Slope Compensation
- Built-in Line & Inductance Compensation for CC Operation
- Built-in Protections with Auto Recovery:

VCC Under Voltage Lockout (UVLO)
VCC Over Voltage Protection (OVP)
On-Chip Thermal Shutdown (OTP)
Cycle-by-Cycle Current Limiting
Over Load Protection (OLP)
Short Circuit Protection (SCP)
Leading Edge Blanking (LEB)
CS Pin Float Protection

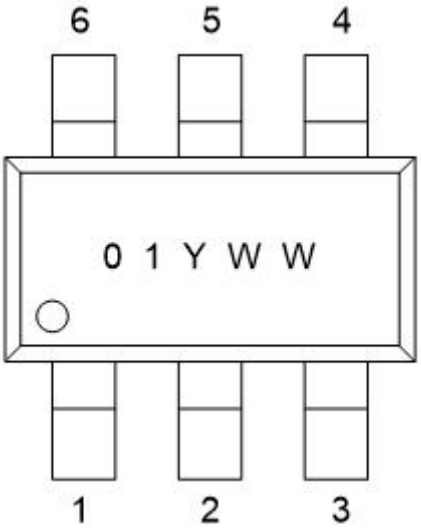
Typical Application



Ordering Information

Part Number	Package	Package Method	Marking
CT5601（SOT23-6）	SOT23-6	Tape 3,000pcs/Roll	01YWW

Pin Assignment



Pin Description

Pin	Pin Name	Description
1	GND	The ground of the IC
2	FB	Feedback pin. The loop regulation is achieved by connecting a photo-coupler to this pin. PWM duty cycle is determined by this pin voltage and the current sense signal at Pin 4
3	SEL	Connect a capacitor (typically value is 10-47nF) between SEL and GND to make the IC work in CC/CV mode. If SEL pin is floated, the IC will work in CV mode only
4	CS	Current sense input pin
5	VCC	IC power supply pin
6	GATE	Totem-pole gate driver output to drive the external MOSFET

Absolute Maximum Ratings

Parameter	Symbol	Parameter Range	Unit
VCC DC Supply Voltage	V_{VCC}	30	V
VCC DC Clamp Current	I_{VCC_Clamp}	10	mA
GATE pin	V_{GATE}	20	V
CS/FB/SEL Voltage range	$V_{CS}/V_{FB}/V_{SEL}$	-0.3 to 7	V
Thermal Resistance Junction-ambient	Rthj-a	250	℃/W
Operating Junction Temperature	T_J	-40～150	℃
Storage Temperature Range	T_{STG}	-55～150	℃
VESD_HBM	Human Body Model	3,000	V
VESD_MM	Machine Model	250	V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability。

Recommended Operation Conditions

Parameter	Value	Unit
Supply Voltage, V_{CC}	10 to 28	V
Operating Ambient Temperature	-40 to 85	℃

Note2. The device is not guaranteed to function outside its operating conditions.

Electronic Characteristics

T_C=25°C,V_{CC} = 18V,unless otherwise specified

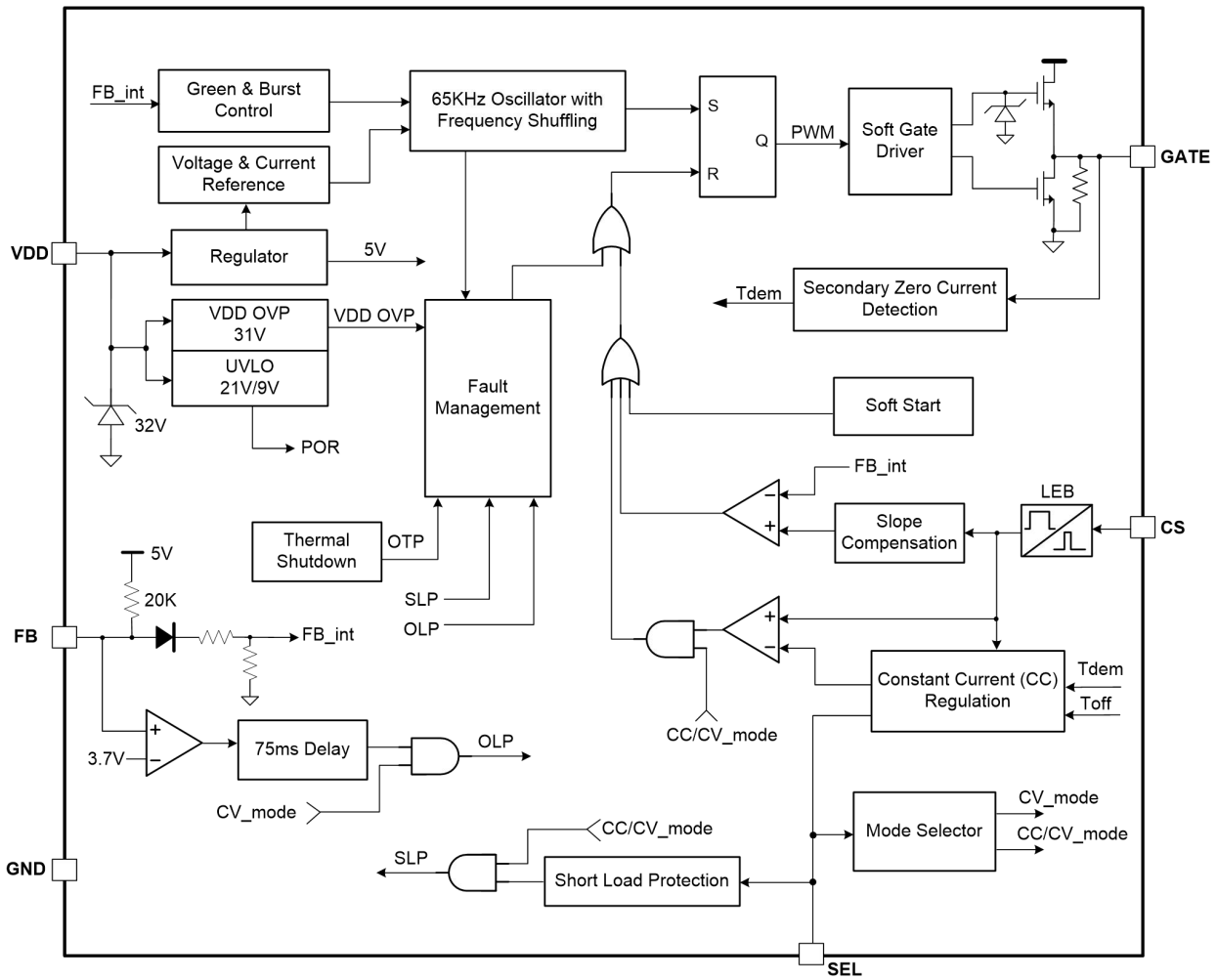
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Section(V_{CC} Pin)						
I_{VCC_st}	Start-up current into VCC pin			2	20	uA
I_{VCC_Op}	Operation Current	V_{FB}=3V,GATE=1nF		1.2	2	mA
$I_{VCC\_standby}$	Standby Current			0.6	1	mA
V_{CC_ON}	VCC Under Voltage Lockout Exit		19	21	21.5	V
V_{CC_OFF}	VCC Under Voltage Lockout Enter		8	9	10	V
V_{CC_OVP}	VCC OVP Threshold		29	31	33	V
V_{CC_Clamp}	VCC Zener Clamp Voltage	I(VCC) = 7 mA	33	35	37	V

Control Function Section (FB Pin)						
V_{FB_Open}	FB Open Voltage			5.9		V
I_{FB_Short}	FB Short Circuit Current	Short FB Pin to GND, Measure Current		0.3		mA
Z_{FB_IN}	FB Input Impedance			20		KΩ
A_{CS}	PWM Gain	$\Delta V_{FB}/\Delta V_{CS}$		2.0		V/V
V_{skip}	FB Under Voltage GATE Clock is OFF			1.0		V
V_{TH_OLP}	Power Limiting FB Threshold Voltage			3.6		V
T_{D_OLP}	Power Limiting Debounce Time	SEL Pin is floating		75		ms
Current Sense Input Section (CS Pin)						
T_{LEB}	CS Input Leading Edge Blanking Time			250		ns
$V_{cs(max)}$	Current limiting threshold		0.97	1.0	1.03	V
T_{D_OC}	Over Current Detection and Control Delay	GATE=1nF		70		ns
Oscillator Section						
F_{OSC}	Normal Oscillation Frequency		60	65	70	KHz
$\Delta F(shuffle)/F_{OSC}$	Frequency Shuffling Range		-4		4	%
T(shuffle)	Frequency Shuffling Period			32		ms
D_{MAX}	Maximum Switching Duty Cycle			66.7		%
F_{Bust}	Burst Mode Base Frequency			22		KHz
CC Loop Regulation Section (SEL = Capacitor)						
$V_{CC\_Reg\_SEL}$	Internal Reference for CC Loop Regulation		194	200	206	mV
$I_{CC\_SEL\_Source}$	Internal Source Current for CC Loop Regulation			20		uA
$V_{CC\_SLP\_SEL}$	Short Load Protection (SLP) Threshold			0.7		V
$T_{CC\_Short\_SEL}$	Short Load Protection (SLP) Debounce Time			210		ms

Driver Section (GATE Pin) (Note 3)						
V_{OL}	Output Low Level	Igate_sink=20mA			1	V
V_{OH}	Output High Level	Igate_source=20 mA	7.5			V
V_{G_Clamp}	Output Clamp Voltage Level	VCC=24V		13		V
T_r	Output Rising Time	GATE=1nF		150		ns
T_f	Output Falling Time	GATE=1nF		60		ns
On-Chip Thermal Shutdown						
T_{SD}	Thermal Shutdown	(Note 3)		165		°C
T_{RC}	Thermal Recovery	(Note 3)		140		°C

Note3. Guaranteed by the Design.

Functional Block Diagram



Applications Information

Operation Description

The CT5601 is a high performance current mode PWM controller for offline flyback charger, motor driver power supply, and adapter applications. The CT5601 has built-in General Primary Side CC control, which simplifies isolated power supply design that requires CC regulation of the output.

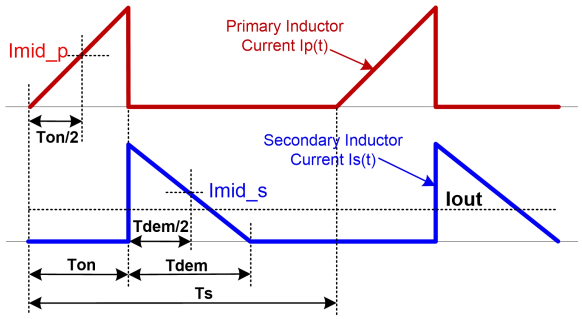
System Start-Up Operation

Before the CT5601 starts to work, it consumes only startup current (typically 2uA) which allows a large value startup resistor to be used to minimize the power loss and the current flowing through the startup resistor charges the VCC hold-up capacitor from the high voltage DC bus. When VCC reaches turn on threshold VCC_ON (typical 21V), The CT5601 begins switching and the IC operation current is increased to be 1.2mA (typical). The hold-up capacitor continues to supply VCC before the auxiliary winding of the transformer takes the control of VCC voltage. When the CT5601 enters into burst mode, it operation current will decrease further, thus less than 75mW standby power can be achieve in sub 30W applications.

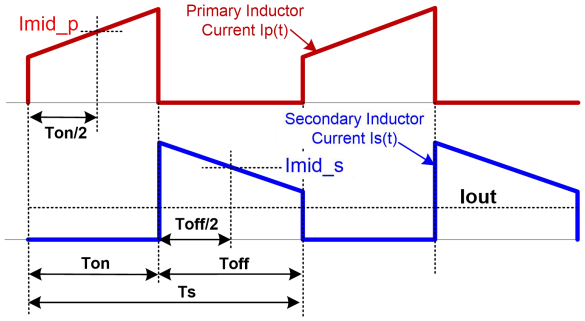
General Primary Side Constant Current Modulation for DCM/CCM

Compared to conventional flyback DCM Primary Side Regulation (PSR) Constant Current (CC) method, a General Primary Side Constant Current Modulation algorithm is adopted in CT5601, which supports transformer DCM and CCM operation simultaneously.

The Fig. on the right illustrates the key waveform of a flyback converter operating in DCM and CCM, respectively. The output current Iout of each mode is estimated by calculating the average current of secondary or primary inductor over one switching cycle:



Waveform of DCM Flyback Converter



Waveform of CCM Flyback Converter

$$I_{OUT} = \frac{\int_0^{T_S} I_S(t)dt}{T_S} = N \times \frac{\int_0^{T_S} I_P(t)dt}{T_S} \quad (1)$$

In Eq(1) above, Is(t) is the secondary inductor or rectification diode current, Ip(t) is the primary inductor current, N is primary-to-secondary transformer turn ratio.

The average secondary inductor current in both DCM and CCM can be expressed in a same form, as a product of secondary inductor discharge time TDIS and secondary inductor current at the middle of TDIS, such as:

$$\int_0^{T_S} I_S(t)dt = I_{mid\_S} \times T_{DIS} = N \times I_{mid\_P} \times T_{DIS} \quad (2)$$

In Eq.(2), Imid_S and Imid_P are the secondary and primary inductor current at the middle of

TDIS and TON respectively, as shown in Fig. Above. TDIS can be given by the following equation:

$$T_{DIS} = \begin{cases} T_{DEM} & (\text{for DCM mode}) \\ T_{OFF} & (\text{for CCM mode}) \end{cases} \quad (3)$$

In Eq(3), TDIS=TDEM for DCM operation and TDIS=TOFF for CCM operation respectively. Combined with Eq.(1) to Eq. (3), the average output current Iout can be expressed as:

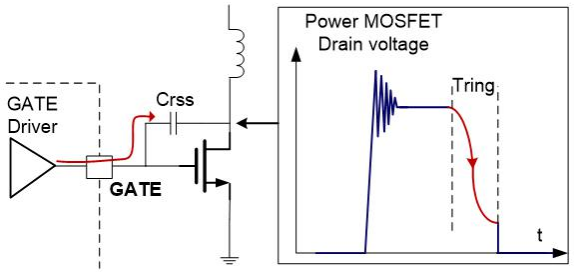
$$I_{OUT} = N \times I_{mid\_P} \times \frac{T_{DIS}}{T_S} = N \times \frac{V_{mid\_P}}{R_{CS}} \times \frac{T_{DIS}}{T_S} \quad (4)$$

In Eq(4), Rcs is the sensing resistor connected between the power MOSFET source to GND. Vmid_P is sampled RCS voltage at the middle of primary power MOSFET conduction time. In CT5601, the product of Vmid_P and TDIS is kept constant by the IC's internal PWM CC regulation loop. The switching frequency is trimmed to 65KHz in CT5601. Therefore, the average output current Iout will be well regulated and given by:

$$I_{CC\_OUT}(mA) = N \times \frac{V_{CC\_Reg}}{Rcs} \cong N \times \frac{200mV}{Rcs(\Omega)} \quad (5)$$

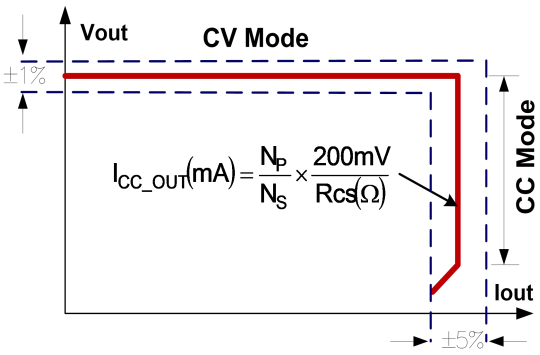
Demagnetization Detection without Auxiliary Winding

In CT5601, the transformer core demagnetization is detected by monitoring the coupling current flowing through the parasitic capacitor Crss between the drain and gate of power MOSFET. When the transformer is fully demagnetized, the drain voltage evolution is governed by the resonating energy transfer between the transformer inductor and the parasitic capacitance of the drain. These voltage oscillations create current oscillation in the parasitic capacitor Crss. A negative current takes place during the decreasing part of the drain oscillation, and a positive current during the increasing part. The transformer demagnetization time corresponds to the inversion of the current by detecting this point, as shown in Fig. on the right.



Mode Selection for CV and CC/CV

The load of SEL pin determines the operation mode. The CT5601 will work in CC/CV mode if an external capacitor is connected between SEL pin and GND. Otherwise, if SEL pin is floating, the IC will work in only CV mode.



±5% CC Regulation, ±1% CV Regulation with Fast Dynamic Response

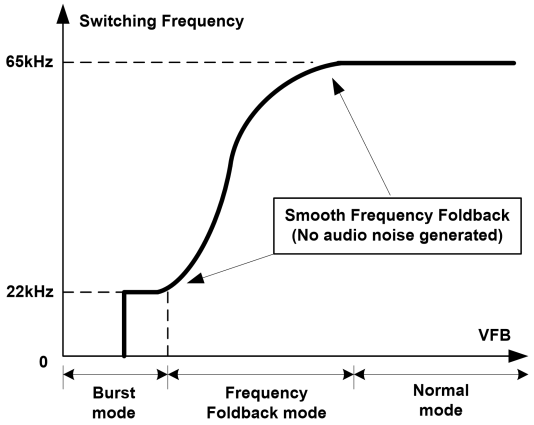
The CC algorithm in The CT5601 compensates line variation and transformer inductance tolerance. The IC can achieve ±5% CC regulation. The CT5601can also achieve ±1% CV regulation and fast dynamic response , due to the same control method as convention PWM controllers.

Oscillator with Frequency Shuffling

PWM switching frequency in CT5601 is fixed to 65KHz and is trimmed to tight range. To improve system EMI performance. The CT5601 operates the system with 4% frequency shuffling around setting frequency.

Green Mode Operation

Since the main power dissipation at light/zero load in a switching mode power supply is from the switching loss which is proportional to the PWM switching frequency. To meet green mode requirement, it is necessary to reduce the switching cycles under such conditions either by skipping some switching pulses or by reducing the switching frequency.

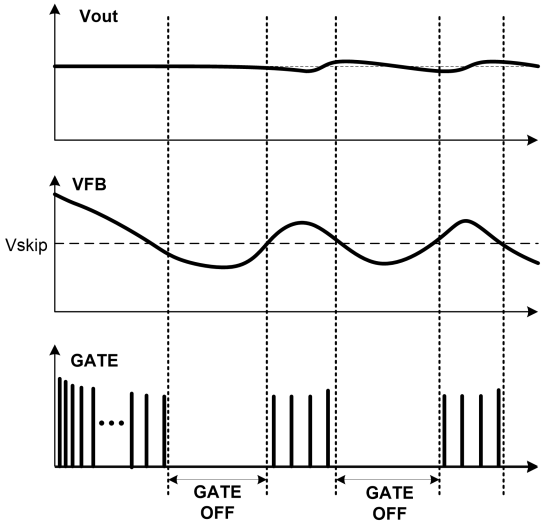


Smooth Frequency Foldback

In CT5601, a Proprietary “Smooth Frequency Foldback” function is integrated to foldback the PWM switching frequency when the loading is light. Compared to the other frequency reduction implementations, this technique can reduce the PWM frequency smoothly without audible noise.

Burst Mode Control

When the loading is very small, the system enters into burst mode. When VFB drops below Vskip, The CT5601 will stop switching and output voltage starts to drop , as shown in Fig. on the right, which causes the VFB to rise. Once VFB rises above Vskip, switching resumes. Burst mode control alternately enables and disables switching, thereby reducing switching loss in standby mode.



Built-in Slope Compensation

In the conventional application, the problem of the stability is a critical issue for current mode controlling, when it operates in higher than 50% of the duty-cycle. In CT5601 the slope compensation circuit is integrated by adding voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Leading Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs across the sensing resistor. The spike is caused by primary side capacitance and secondary side rectifier reverse recovery. To avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period (250ns, typical), the PWM comparator is disabled and cannot switch off the gate driver.

On Chip Thermal Shutdown (OTP)

When the CT5601's temperature is over 165℃, the CT5601 will shut down. Only when the temperature drops to 140℃, the CT5601 will restart.

Soft Start

The CT5601 features an internal 2ms (typical) soft start that slowly increases the threshold of cycle-by-cycle current limiting comparator during start-up sequence. It helps to prevent transformer saturation and reduce the stress on the secondary diode during start-up. Every restart attempt is followed by a soft start activation.

Constant Power Limiting in CV Mode

In CV mode, a proprietary "Constant Power Limiting" block is integrated to achieve constant maximum output power capability over universal AC input range. Based on the duty cycle information, the CT5601generates OCP threshold according to a proprietary analog algorithm.

Short Circuit Protection (SCP) in CC/CV Mode

In CT5601, if the IC works in CC/CV mode and CC voltage is below 0.7V, the CT5601 will enter into Short Circuit Protection (SCP) mode, in which the CT5601 will enter into auto recovery protection mode.

Over Load Protection (OLP) in CV Mode

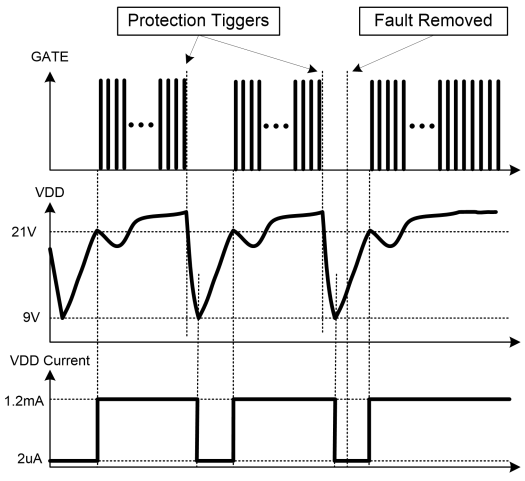
In CV mode and if over load occurs, a fault is detected. If this fault is present for more than 75ms (typical), the protection will be triggered, the IC will experience an auto-recovery mode protection as mentioned above. The 75ms delay time is to prevent the false trigger from the power-on and turn-off transient.

VCC Over Voltage Protection (OVP) and Zener Clamp

When VCC voltage is higher than 31V (typical), the IC will stop switching. This will cause VCC fall down to be lower than $VCC_{\_OFF}$ (typical 9V) and then the system will restart up again. An internal 35V (typical) zener clamp is integrated to prevent the IC from damage.

CS Pin Float Protection

When VCC voltage is higher than $VCC_{\_ON}$ (21V typical), IC firstly starts to check whether CS pin is floated. If CS pin is floated, switching is blocked and IC enters auto-recovery mode; otherwise, normal work begins. With this protection, system stability is enhanced.



Auto Recovery Mode Protection

As shown in Fig. on the right, once a fault condition is detected, PWM switching will stop. This will cause VCC to fall because no power is delivered form the auxiliary winding. When VCC falls to $VCC_{\_OFF}$ (typical 9V), the protection is reset and the operating current reduces to the

startup current, which causes VCC to rise. The system begins switching when VCC reaches to $VCC_{\_ON}$ (typical 21V). However, if the fault still exists, the system will experience the above mentioned process. If the fault has gone, the system resumes normal operation. In this manner, the auto restart can alternatively enable and disable the switching until the fault condition is disappeared.

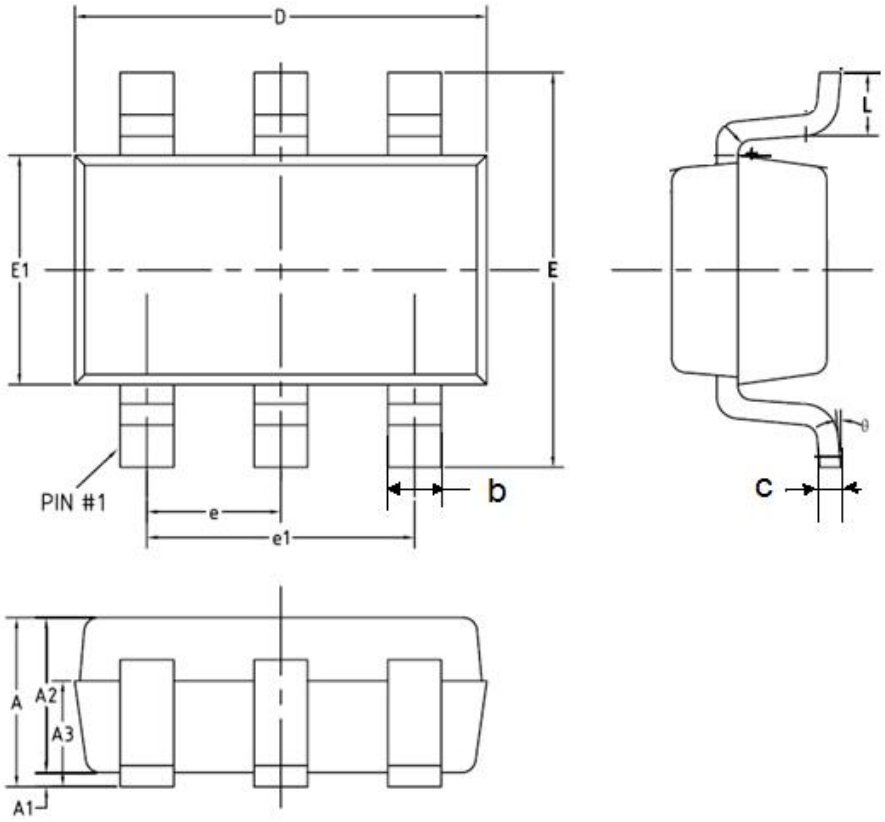
Soft Gate Driver

The output stage of the CT5601 is a totem-pole gate driver with 400mA capability. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. An internal 13V clamp is added for MOSFET gate protection at higher than expected VCC input. A soft driving waveform is implemented to minimize EMI.

SOT23-6 封装机械尺寸
SOT23-6 MECHANICAL DATA

单位:毫米/UNIT：mm

符号/SYMBOL	最小值/min	典型值/nom	最大值/max
A	0.90		1.45
A1	0		0.15
A2	0.90		1.30
A3	0.60		0.70
b	0.35		0.49
C	0.08		0.22
D	2.80		3.00
E	2.60		3.00
E1	1.50		1.70
e	0.85		1.05
e1	1.85		2.00
L	0.35		0.60
θ	0		8°



Revision history

Revision	Release data	Description
1.0	2016-12-28	Initial Version