General Description

The CT5600 is a high performance Primary Side Regulation (PSR) controller with high precision CV/CC control ideal for charger applications.

In CV mode, the CT5600 adopts Multi Mode Control which uses the hybrid of AM (Amplitude Modulation) mode and (Frequency Modulation) FM mode to improve system efficiency and reliability. In CC mode, the CT5600 uses PFM control with line and load CC compensation. The CT5600 can achieve audio noise free operation and optimized dynamic response. The built-in Cable Drop Compensation (CDC) function can provide excellent CV performance.

The CT5600 integrates functions and protections of Under Voltage Lockout (UVLO), VCC over Voltage Protection (VCC OVP), Cycle-by-cycle Current Limiting (OCP), Short Load Protection (SLP), Gate Clamping, and VCC Clamping.

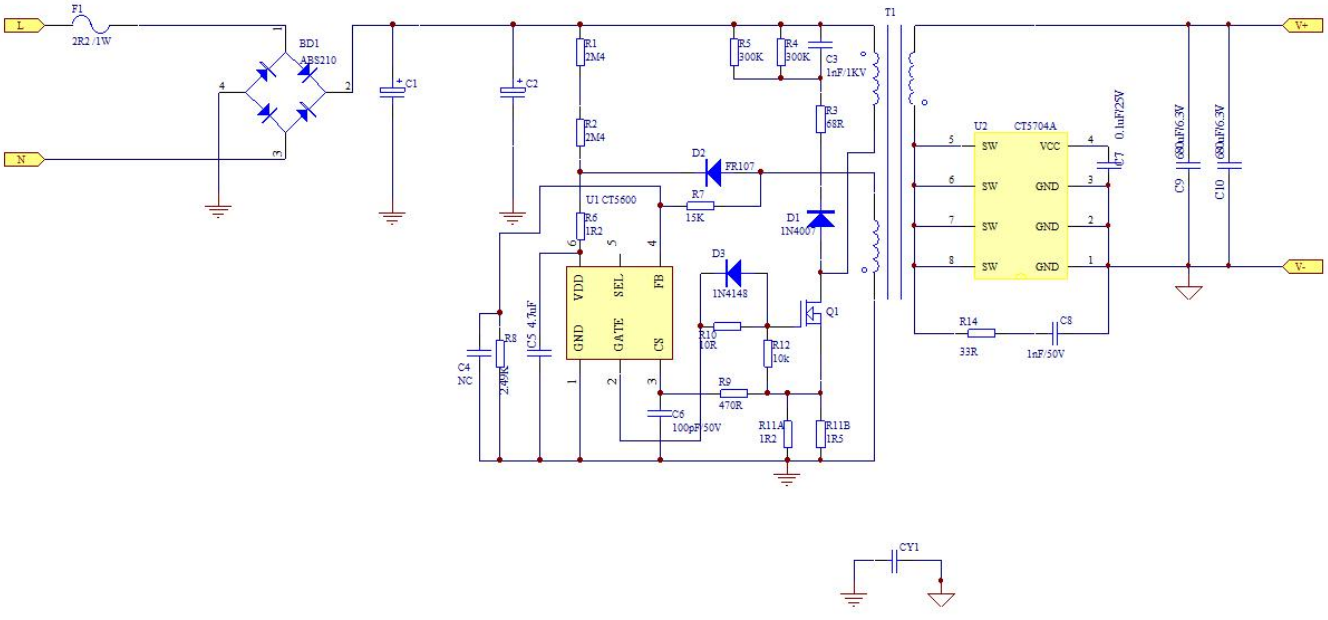
The CT5600 is available in SOT23-6 package.

Features

- Multi Mode PSR Control
- Audio Noise Free Operation for PSR
- Optimized Dynamic Response for PSR
- Low Standby Power <70mW
- ±4% CC and CV Regulation
- Programmable Cable Drop Compensation (CDC) in PSR CV Mode
- Built-in AC Line & Load CC Compensation
- Build in Protections:
  - Short Load Protection (SLP)
  - On-Chip Thermal Shutdown (OTP)
  - Cycle-by-Cycle Current Limiting
  - Leading Edge Blanking (LEB)
  - Pin Floating Protection

  VCC OVP & UVLO & Clamp

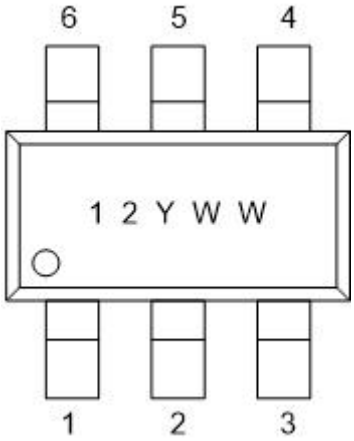
Typical Application



Ordering Information

Part Number	Package	Package Method	Marking
CT5600（SOT23-6）	SOT23-6	Tape 3,000pcs/Roll	12YWW

Pin Assignment



Pin Description

Pin	Pin Name	Description
1	GND	The Ground of the IC
2	GATE	Gate Driver for External MOSFET Switch
3	CS	Current Sense Input Pin
4	FB	System feedback pin which regulates both the output voltage in CV mode and output current in CC mode based on the flyback voltage of the auxiliary winding
5	NC	This BIN should be floating
6	VCC	Power Supply Pin of the Chip

Absolute Maximum Ratings

Parameter	Symbol	Parameter Range	Unit
VCC DC Supply Voltage	V_{VCC}	34.5	V
VCC DC Clamp Current	I_{VCC_Clamp}	10	mA
GATE pin	V_{GATE}	20	V
CS Voltage range	V_{CS}	-0.3 to 7	V
FB voltage range	V_{FB}	-0.7 to 7	V
Thermal Resistance Junction-ambient	Rthj-a	250	℃/W
Operating Junction Temperature	T_J	-40～150	℃
Storage Temperature Range	T_{STG}	-55～150	℃
VESD_HBM	Human Body Model	2,000	V
VESD_MM	Machine Model	200	V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability。

Recommended Operation Conditions

Parameter	Value	Unit
Supply Voltage, V_{CC}	11 to 27	V
Operating Ambient Temperature	-40 to 85	℃
Maximum Switching Frequency @ Full Loading	70	kHz
Minimum Switching Frequency @ Full Loading	35	kHz

Note2. The device is not guaranteed to function outside its operating conditions.

Electronic Characteristics

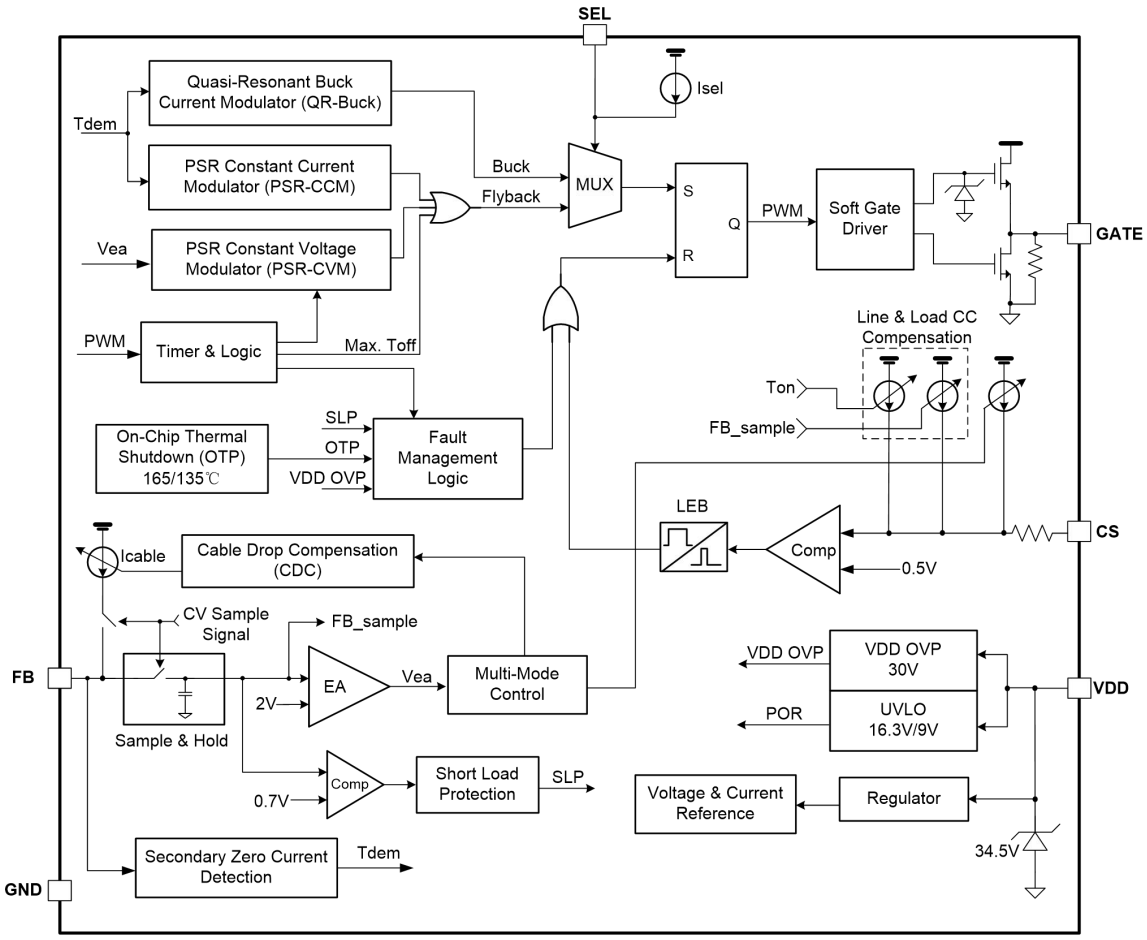
T_C =25℃,V_{CC} = 18V,unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Section(V_{CC} Pin)						
I_{VCC_st}	Start-up current into VCC pin			2	15	uA
I_{VCC_Op}	Operation Current	V_{FB}=1.1V, V_{CC}=18V	0.3	0.7	0.9	mA
$I_{VCC\_standby}$	Standby Current			0.5	1	mA
V_{CC_ON}	V_{CC} Under Voltage Lockout Exit		15	16.3	17.5	V
V_{CC_OFF}	V_{CC} Under Voltage Lockout Enter		8	9	10	V

V_{CC_OVP}	V_{CC} OVP Threshold		28	30	32	V
V_{CC_Clamp}	V_{CC} Zener Clamp Voltage	$I(V_{CC})$ = 7mA	32.5	34.5	36.5	V
Control Function Section (FB Pin)						
V_{FB_REF}	Internal Error Amplifier (EA) Reference Input		1.97	2.0	2.03	V
V_{FB_SLP}	Short Load Protection (SLP) Threshold			0.7		V
T_{FB_Short}	Short Load Protection (SLP) Debounce Time			10		ms
V_{FB_DEM}	Demagnetization Comparator Threshold			25		mV
T_{off_min}	Minimum OFF time	(Note 3)		2		us
T_{off_max}	Maximum OFF time		3.6	4	4.5	ms
I_{Cable_max}	Maximum Cable Drop compensation current		48	53	58	uA
Current Sense Input Section (CS Pin)						
T_{LEB}	CS Input Leading Edge Blanking Time			500		ns
$V_{cs(max)}$	Current limiting threshold		490	500	510	mV
T_{D_OCP}	Over Current Detection and Control Delay	GATE=0.5nF		100		ns
GATE Driver Section (GATE Pin) (Note 3)						
V_{G_Clamp}	Output Clamp Voltage Level	VCC=24V		16		V
T_r	Output Rising Time	GATE=0.5nF		700		ns
T_f	Output Falling Time	GATE=0.5nF		40		ns
Flyback or Buck Selection Section (SEL Pin)						
$V_{SEL(floating)}$	SEL Pin Floating Voltage	(Note 3)		5.7		V
I_{SEL}	Internal SEL Pin Pull up Current	(Note 3)		35		uA
Over Temperature Protection						
T_{SD}	Thermal Shutdown	(Note 3)	---	165	--	℃

Note3. Guaranteed by the Design.

Functional Block Diagram



Applications Information

Operation Description

The CT5600 is a high performance, multi mode, highly integrated DCM (Discontinuous Conduction Mode) Primary Side Regulation (PSR) controller. The built-in high precision CV/CC control with high level protection features makes it suitable for offline small power converter applications.

System Start-Up Operation

Before the IC starts to work, it consumes only startup current (typically 2uA) which allows a large value startup resistor to be used to minimize the power loss and the current flowing through the startup resistor charges the VDD hold-up capacitor from the high voltage DC bus. When VDD reaches UVLO turn-on voltage of 16.3V (typical), CT5600 begins switching and the IC operation current is increased to be 1mA (typical). The hold-up capacitor continues to supply VDD before the auxiliary winding of the transformer takes the control of VDD voltage.

Once CT5600 enters very low frequency FM (Frequency Modulation) mode, the operating current is reduced to be 0.5mA typically, which helps to reduce the standby power loss.

PSR Constant Voltage Modulation (PSR-CVM)

In primary side control, the output voltage is sensed on the auxiliary winding during the transfer of transformer energy to the secondary. The CV sampling signal timing waveform in CT56002. As shown in Fig.1, it is clear that there is a down slope representing a decreasing total rectifier Vf and its voltage drop as the secondary current decreases to zero. To achieve an accurate representation of the secondary output voltage on the auxiliary winding, the CV sampling signal blocks the leakage inductance reset and ringing. When the CV sampling process is over, the internal sample/hold (S&H) circuit captures the error signal and amplifies it through the internal Error Amplifier (EA). The output of EA is sent to the Primary Side Constant Voltage Modulator (PS-CVM) for CV control. The internal reference voltage for EA is trimmed to 2V with high accuracy.During the CV sampling process, an internal variable current source is flowing to FB pin for Cable Drop Compensation (CDC). Thus, there is a step at FB pin in the transformer demagnetization process, as shown in Fig.1. Fig.1 also illustrates the equation for “demagnetization plateau”, where Vo and VF is the output voltage and diode forward voltage; R1 and R2 is the resistor divider connected from the auxiliary winding to FB Pin, Ns and Na are secondary winding and auxiliary winding respectively.

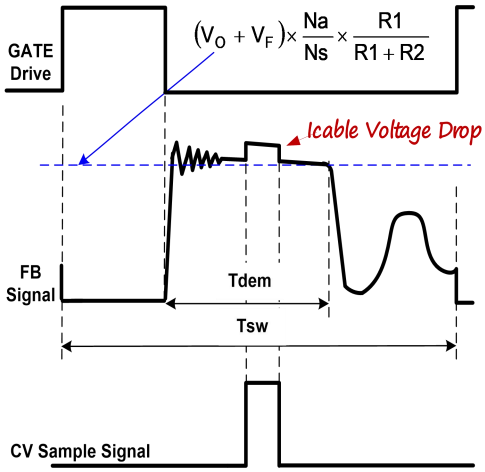


Fig.1

When system enters over load condition, the output voltage falls down and the FB sampled voltage should be lower than 2V internal reference which makes system enter CC Mode automatically.

PSR Constant Current Modulation (PSR-CCM)

Timing information at the FB pin and current information at the CS pin allow accurate regulation of the secondary average current. The control law dictates that as power is increased in CV regulation and approaching CC regulation the primary peak current is at Ipp(max), as shown in Fig.2.

Referring to Fig.2 above, the primary peak current, transformer turns ratio, secondary demagnetization time (Tdem), and switching period (Tsw) determines the secondary average output current Iout. Ignoring leakage inductance effects, the equation for average output current is shown in Fig.2. When the average output current Iout reaches the regulation reference in the Primary Side Constant Current Modulator (PS-CCM) block, the IC operates in pulse frequency modulation (PFM) mode to control the output current at any output voltage at or below the voltage regulation target as long as the auxiliary winding can keep VDD above the UVLO turn-off threshold.

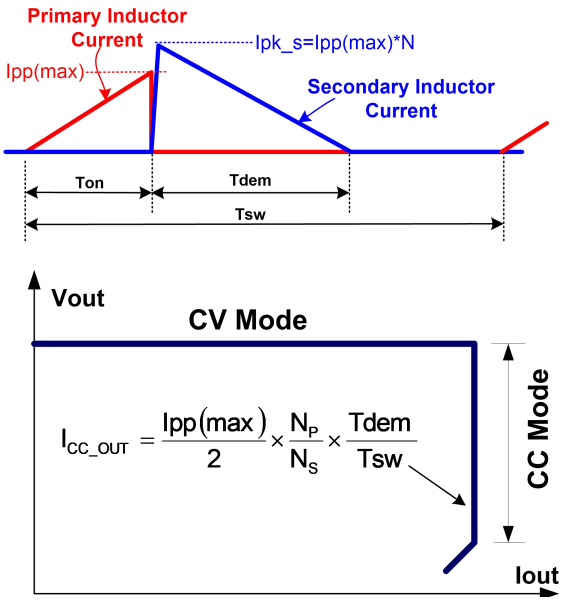


Fig. 2

In CT5600, the ratio between Tdem and Tsw in CC

mode is 1/2. Therefore, the average output current can be expressed as:

$$I_{PSR\_CC\_OUT}(mA) \cong \frac{1}{4} \times N \times \frac{500mV}{Rcs(\Omega)}$$

In the equation above,

N---The turn ratio of primary side winding to secondary side winding.

Rcs--- the sensing resistor connected between the power MOSFET source to GND.

Multi Mode Control in CV Mode

To meet the tight requirement of averaged system efficiency and no load power consumption, a hybrid of frequency modulation (FM) and amplitude modulation (AM) is adopted in CT5600 which is shown in the Fig 3.

Around the full load, the system operates in FM mode. When normal to light load conditions, the IC operates in FM+AM mode to achieve excellent regulation and high efficiency. When the system is near zero loading, the IC operates in FM again for standby power reduction. In this way, the no-load consumption can be less than 70mW.

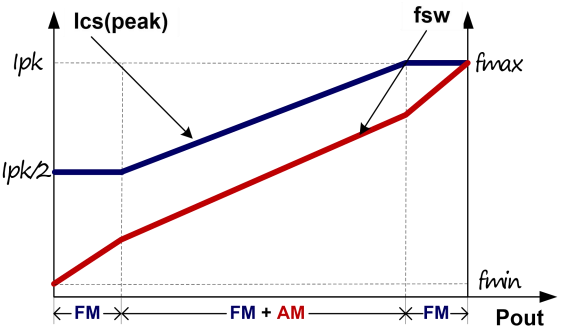


Fig.3

Programmable Cable Drop Compensation (CDC) in CV Mode

In smart phone charger application, the battery is always connected to the adapter with a cable wire which can cause several percentages of voltage drop on the actual battery voltage. In CT5600, an offset voltage is generated at FB pin by an internal current source (modulated by CDC block, as shown in Fig.4) flowing into the resistor divider. The current is proportional to the switching period, thus, it is inversely proportional to the output power Pout. Therefore, the drop due the cable loss can be compensated. As the load decreases from full loading to zero loading, the offset voltage at FB pin will increase. By adjusting the resistance of R1 and R2 (as shown in Fig.4), the cable loss compensation can be programmed. The percentage of maximum compensation is given by

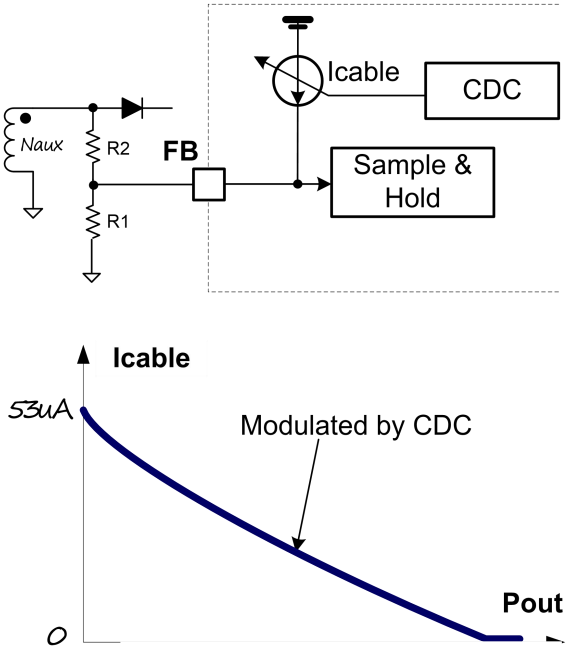


Fig.4

$$\frac{\Delta V(cable)}{Vout} \approx \frac{Icable\_max \times (R1//R2)}{V_{FB\_REF}} \times 100\%$$

For example,

R1=3 K Ω , R2=18K Ω , The percentage of maximum compensation is given by

$$\frac{\Delta V(cable)}{Vout} = \frac{53uA \times (3K//18K)}{2V} \times 100\% = 8.1\%$$

Optimized Dynamic Response

In CT5600, the dynamic response performance is optimized to meet USB charge requirements.

Audio Noise Free Operation for PSR

As mentioned above, the multi-mode CV control with a hybrid of FM and AM provides frequency modulation. An internal current source flowing to CS pin realizes CS peak voltage modulation. In CT5600, the optimized combination of frequency modulation and CS peak voltage modulation algorithm can provide audio noise free operation from full loading to zero loading.

Short Load Protection (SLP)

In KP212, the output is sampled on FB pin and then compared with a threshold of UVP (0.7V typically) after an internal blanking time (10ms typical).

In KP212, when sensed FB voltage is below 0.7V, the IC will enter into Short Load Protection (SLP) mode, in which the IC will enter into auto recovery protection mode.

VCC Over Voltage Protection (OVP) and Zener Clamp

When VCC voltage is higher than 30V (typical), the IC will stop switching. This will cause VCC fall down to be lower than VCC_OFF (typical 9V) and then the system will restart up again. An internal 34.5V (typical) zener clamp is integrated to prevent the IC from damage.

On Chip Thermal Shutdown (OTP)

When the IC temperature is over 165℃, the IC shuts down. Only when the IC temperature drops to 135℃, IC will restart.

Pin Floating Protection

In CT5600, if pin floating situation occurs, the IC is designed to have no damage to system.

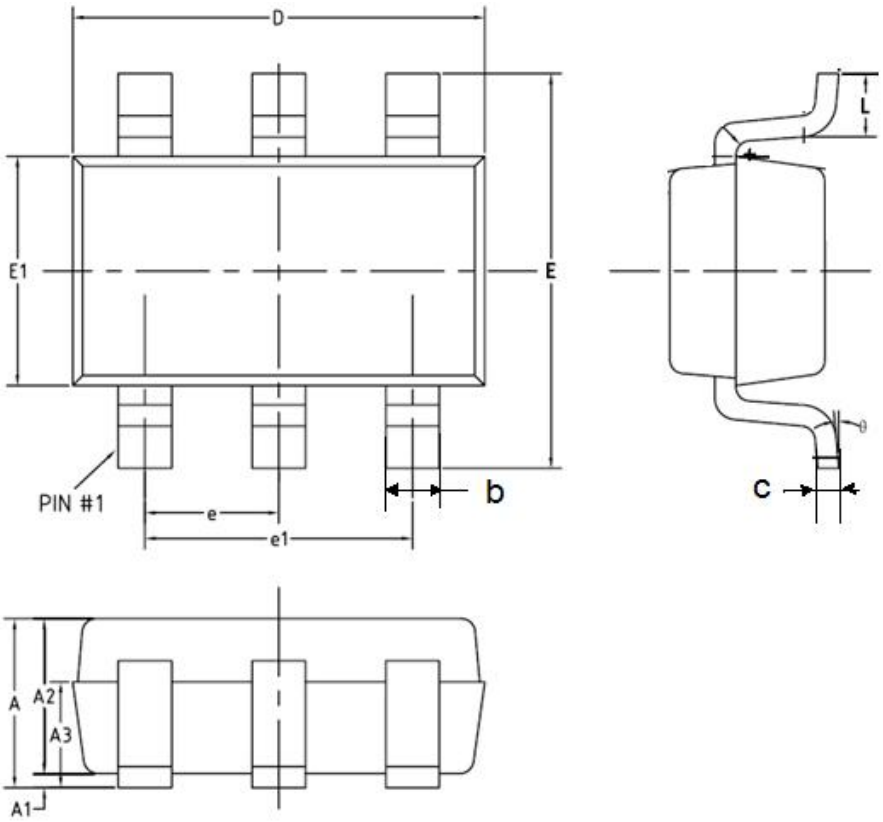
Soft Totem-Pole Gate Driver

The CT5600 has a soft totem-pole gate driver with optimized EMI performance.

SOT23-6 封装机械尺寸
SOT23-6 MECHANICAL DATA

单位:毫米/UNIT：mm

符号/SYMBOL	最小值/min	典型值/nom	最大值/max
A	0.90		1.45
A1	0		0.15
A2	0.90		1.30
A3	0.60		0.70
b	0.35		0.49
C	0.08		0.22
D	2.80		3.00
E	2.60		3.00
E1	1.50		1.70
e	0.85		1.05
e1	1.85		2.00
L	0.35		0.60
θ	0		8°



Revision history

Revision	Release data	Description
1.0	2015-12-1	Initial Version