General Description

The CT5202S8 is a low-cost, constant-current, constant-voltage primary feedback controller. It integrates high-voltage start-up devices and uses patented self-powered technology, which makes the system without startup resistor, power supply winding and power supply diode, greatly reducing production costs. It is suitable for various low power AC/DC chargers and adapters.

In CC control, the current and output power setting can be adjusted externally by the sense resistor Rcs at CS pin. In CV control, multi-mode operations are utilized to achieve high performance and high efficiency. Device operates in (Pulse Frequency Modulation) PFM in CC mode as well at large load condition and it operates in the hybrid of AM (Amplitude Modulation) mode and (Frequency Modulation) FM mode at light/medium load. The chip can achieve audio noise free operation and optimized dynamic response. CT5202S8 has built-in output cable compensation, and the compensation ratio can be adjusted by modifying the resistance value of the feedback resistance to meet the requirements of various output cables.

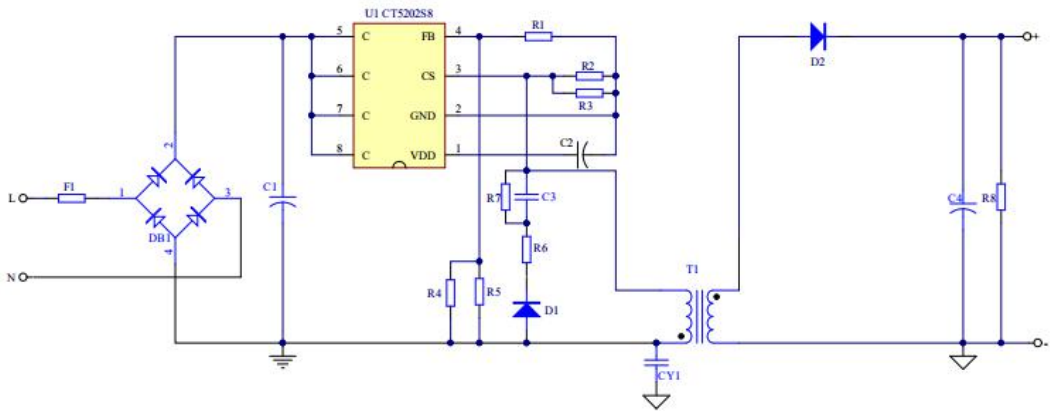
Furthermore, The CT5202S8 features fruitful protections like Open Circuit Protection, Output Short Circuit Protection and Over Temperature Protection to eliminate the external protection circuits and provide reliable operations.

The CT5202S8 is available in SOP-8 package.

Features

- Built-in HV Start-up and IC Power Supply Circuit, Power Supply Winding and Power Supply Diode is Free
- Built-in 850V High Voltage BJT, RCD Snubber could be remove for 5V/1A application
- Quasi-Resonant Primary Side Regulation (QR-PSR) Control with High Efficiency
- Multi-Mode PSR Control
- Fast Dynamic Response
- Built-in Dynamic Base Drive
- Audio Noise Free Operation
- ±5% CC and CV Regulation
- Programmable Cable Drop Compensation (CDC) in CV Mode
- Built-in AC Line & Load CC Compensation
- SOP-8 package better for thermal performance
- Build in Protections:
  - Short Load Protection (SLP)
  - Cycle-by-Cycle Current Limiting (OCP)
  - Leading Edge Blanking (LEB)
  - On-Chip Thermal Shutdown (OTP)
  - VDD OVP & UVP & Clamp

Typical Application

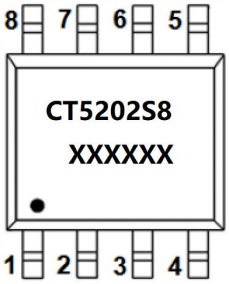


Ordering Information

Part Number	Package	Package Method	Marking
CT5202S8（SOP-8）	SOP-8	Tape 4,000pcs/Roll	CT5202S8 XXXXXX

Pin Assignment

CT5202S8--Part Number；
XXXXXX--Date Code (6 digits)



Pin Description

Pin	Pin Name	Description
VDD	1	IC Supply Voltage input
GND	2	IC Ground
CS	3	Current sense input
FB	4	Feedback input
C	5/6/7/8	Collector of internal BJT

Recommended Operation Conditions

Part Number	230VAC ± 15%(2)	85-265VAC
CT5202S8	6.5W	5W

Note 1. The Max. output power is limited by junction temperature

Note 2. Typical continuous power in a non-ventilated enclosed adapter with sufficient drain pattern as a heat sink at 50℃ ambient.

Absolute Maximum Ratings

Parameter	Symbol	Parameter Range	Unit
C pin Voltage(C)	V_C	-0.3~850	V
Supply Voltage（VDD）	V_{VDD}	-0.3~8	V
FB pin Voltage （FB）	V_{FB}	-0.8~8	V
CS pin voltage （CS）	V_{CS}	-1.5~8	V
OUT pin output current	I_{OUT}	Internal limited	A
Maximum Power Dissipation (Ta=25°C)	P_{tot}	0.45@ SOP-8	W
Thermal Resistance Junction-ambient	Rthj-a	145@ SOP-8	°C/W
Operating Junction Temperature	T_J	-40～150	°C
Storage Temperature Range	T_{STG}	-55～150	°C
V_{ESD_HBM}	Human Body Model	2,000	V
V_{ESD_MM}	Machine Model	200	V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability。

Recommended Operation Conditions

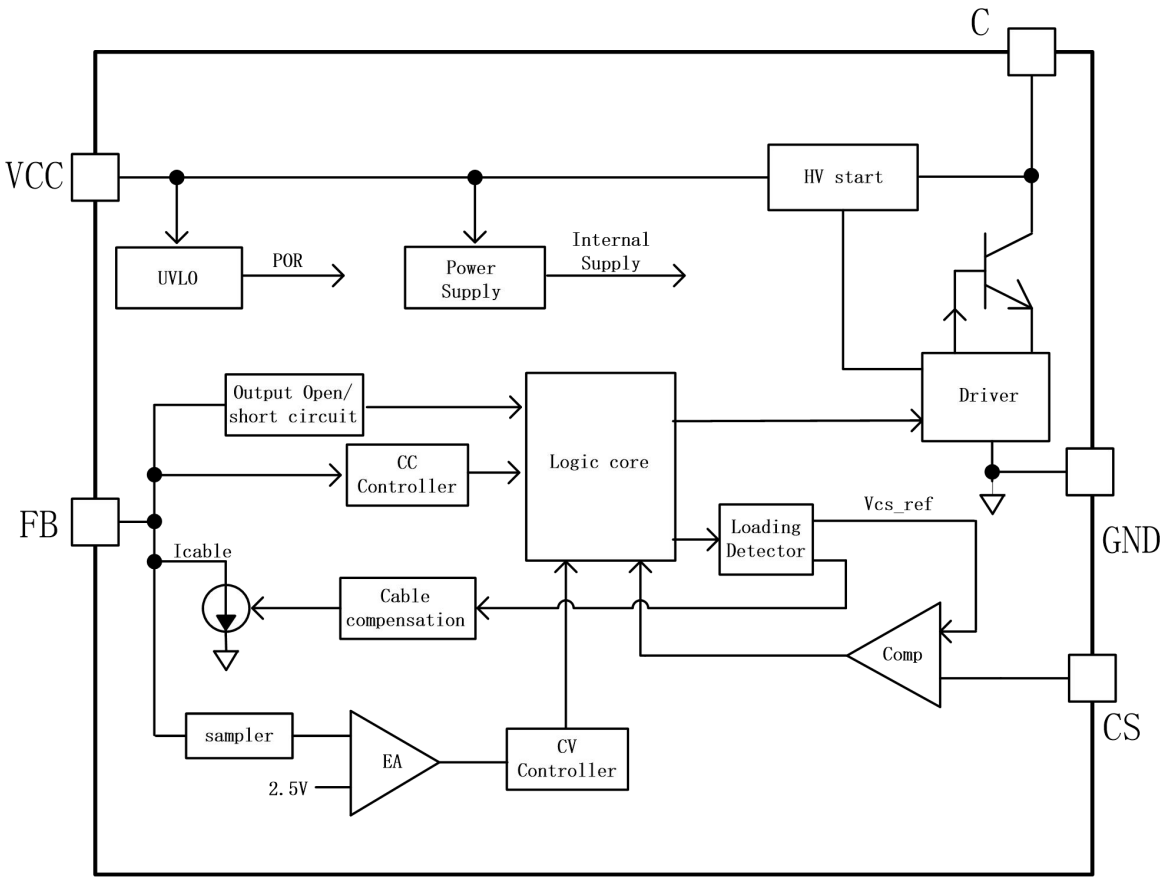
Parameter	Value	Unit
Operating Ambient Temperature	-40 to 85	°C
Maximum Switching Frequency @ Full Loading	70	kHz
Minimum Switching Frequency @ Full Loading	35	kHz

Note2. The device is not guaranteed to function outside its operating conditions.

Electronic Characteristics

T_C =25°C,V_{DD} = 5V,unless otherwise specified						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Supply Voltage Section (V_{DD} Pin)						
V_{DD}_on	Turn-on Voltage	V_{DD} rise		6.5		V
V_{DD}_off	Turn-off Voltage	V_{DD} fall		4.3		V
Control Function Section (FB Pin)						
Vfb_ref	FB Threshold Voltage			2.5		V
Icable_max	Maximum cable compensation current	Full load		18		uA
F_min	Minimum frequency			300		Hz
Vfb_OVP	FB OVP Threshold			3.75		V
Vfb_SCP	FB Short Circuit Threshold			1.4		V
Current Sense Input Section (CS Pin)						
Vcs_th1	Maximum Current Threshold Voltage			1		V
Vcs_th0	Minimum Current Threshold Voltage			0.5		V
T_{LEB}	Leading Edge Blanking Duration			400		ns
Power BJT Section (C Pin)						
BV_{CBO}	Collector-Base Breakdown Voltage		850	-		V
Ic	Maximum Collector Current			2.0		A
On-Chip Thermal Shutdown						
T_Z	Intelligent Thermal Control Threshold	Output Power Shut Down	---	155	--	℃
T_{OTP}	OTP Threshold	Restart		140	--	℃

Functional Block Diagram



Applications Information

Functional Description

The CT5202S8 is a high performance, highly integrated DCM (Discontinuous Conduction Mode) Primary Side Regulation (PSR) controller. The patented self-powered technology is used, so that the system can achieve high precision voltage output without start-up resistance, power supply winding, power supply diode, opto-coupler and TL431. It is suitable for various low power AC/DC chargers and adapters.

System Start-Up Operation

The CT5202S8 built-in High voltage start-up device. After the system is powered on, the high voltage Pin charges the VCC capacitor. When the VCC voltage reaches the start-up voltage of the chip, the internal control circuit of the chip starts to work.

In order to provide a stable working voltage for the chip, it is suggested that the bypass capacitor of VCC pin should be low ESR capacitor to ensure the reliable and stable operation of the chip

and the small ripple of VCC power supply. It is recommended that the electrolytic capacitor with good temperature characteristics of 22uF be used.

The ESR of capacitor increases exponentially at low temperature, in order to avoid the difficulty of starting at low temperature, ***a ceramic chip capacitor of about 1uF X7R material is needed to be connected in parallel to VDD pins.***

Constant Output Voltage Settings

The CT5202S8 captures the primary winding feedback voltage at FB pin and operates in constant-voltage (CV) mode to regulate the output Voltage. Assuming the secondary winding is master, the primary winding is slave during the D1 on-time. The primary voltage is given by:

$$V_{\text{Primary}} = \frac{N_P}{N_S}(V_O + V_d)$$

Where Vd is the diode forward drop voltage, N_P is the turns of primary winding, and N_S is the turns of secondary winding.

Via a resistor divider connected between the Primary winding and FB (pin 4), the Primary voltage is sampled at the portion of Tons after D1 is turned on and it is hold until the next sampling. The sampled voltage is compared with Vfb_ref (typical 2.5V) and the error is amplified. The error amplifier output reflects the load condition and controls the switching off time to regulate the output voltage, thus constant output voltage can be achieved.

When the sampled voltage is below Vfb_ref and the error amplifier output reaches its minimum, the switching frequency is controlled by the sampled voltage to regulate the output current, thus the constant output current can be achieved. The output voltage is given by:

$$Vo = \frac{2.5 \times (R_{FBL} + R_{FBH})}{R_{FBL}} \times \frac{N_S}{N_P} - Vd$$

Adjustable CC Point and Output Power

In CT5202S8, the CC point and maximum output power can be externally adjusted by external current sense resistor Rs at CS pin as illustrated in typical application diagram. The larger Rs, the smaller CC point is, and the smaller output power becomes.

In CT5202S8, the CC point output current is given by

$$Io=0.25*Ipk*Np/Ns$$

Where Ipk is the primary peak current, Np is the turns of primary winding, Ns is the turns of secondary winding.

The primary peak current in CC mode is given by:

$$Ipk=1/Rcs$$

Where Rcs is the current sense resistor at CS pin as illustrated in typical application diagram.

Operation Switching Frequency

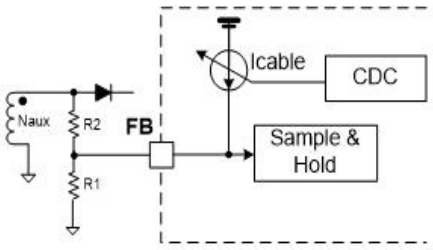
The switching frequency of CT5202S8 is adaptively controlled according to the load conditions and the operation modes. For flyback operating in DCM, The maximum switching frequency is given by

$$F_{\max} = \frac{2 \times P_{O\_MAX}}{\eta \times L_P \times I_{pk}^2}$$

Where P_{O_MAX} is the maximum output power, η is the transfer efficiency, Lp indicate the inductance of primary winding and Ip is the peak current of primary winding.

Programmable Cable Drop Compensation (CDC) in CV Mode

In smart phone charger application, the battery is always connected to the adapter with a cable wire which can cause several percentages of voltage drop on the actual battery voltage. In CT5202S8, an offset voltage is generated at FB pin by an internal current source (modulated by CDC block, as shown in the Fig. as below) flowing into the resistor divider. The current is proportional to the switching period, thus, it is inversely proportional to the output power Pout. Therefore, the drop due the cable loss can be compensated. As the load decreases from full loading to zero loading, the offset voltage at FB pin will increase. By adjusting the resistance of R1 and R2 (as shown in the Fig.), the cable loss compensation can be programmed. The percentage of maximum compensation is given by



$$\frac{\Delta V(\text{cable})}{\text{Vout}} \approx \frac{\text{Icable\_max} \times (\text{R1//R2})}{V_{FB\_REF}} \times 100\%$$

For example, R1=8.2KΩ, R2=300KΩ, The percentage of maximum compensation is given by:

$$\frac{\Delta V(\text{cable})}{\text{Vout}} = \frac{18\text{uA} \times (8.2\text{K}//300\text{K})}{2.5\text{V}} \times 100\% = 5.75\%$$

Output OVP and Short Circuit Protection

When the FB voltage is higher than 3.75V, the chip enters OVP mode. The output OVP voltage is given by:

$$V_{OVP} = \frac{3.75 \times (R_{FBL} + R_{FBH})}{R_{FBL}} \times \frac{N_S}{N_P}$$

When the fb voltage continues below 1.4V, the chip enters short-circuit mode. The output short-circuit voltage is given by:

$$V_{SCP} = \frac{1.4 \times (R_{FBL} + R_{FBH})}{R_{FBL}} \times \frac{N_S}{N_P}$$

Fast Dynamic Response

In CT5202S8, the dynamic response performance is optimized to meet USB charge requirements.

On Chip Thermal Shutdown (OTP)

When the CT5202S8 temperature is over 155℃, the IC shuts down. Only when the IC temperature drops to 140℃, IC will restart.

PCB Layout Consideration

The following rules should be followed in PCB Layout:

The Area of Power Loop: The area of the main current loop should be as small as possible to reduce EMI radiation, such as the primary current loop, the snubber circuit and the secondary rectifying loop. Drain pin increases the copper area of the drain terminal for heat dissipation. And the PCB trace must be wide and short for thermal consideration.

Bypass Capacitor and FB divider resistor:The bypass capacitor on VCC and the FB divider resistor should be placed as close as possible to pin out. And the negative node of VCC capacitor and the FB down resistor should be connected directly to the IC GND pin before single point connected to the negative node of the output capacitor.

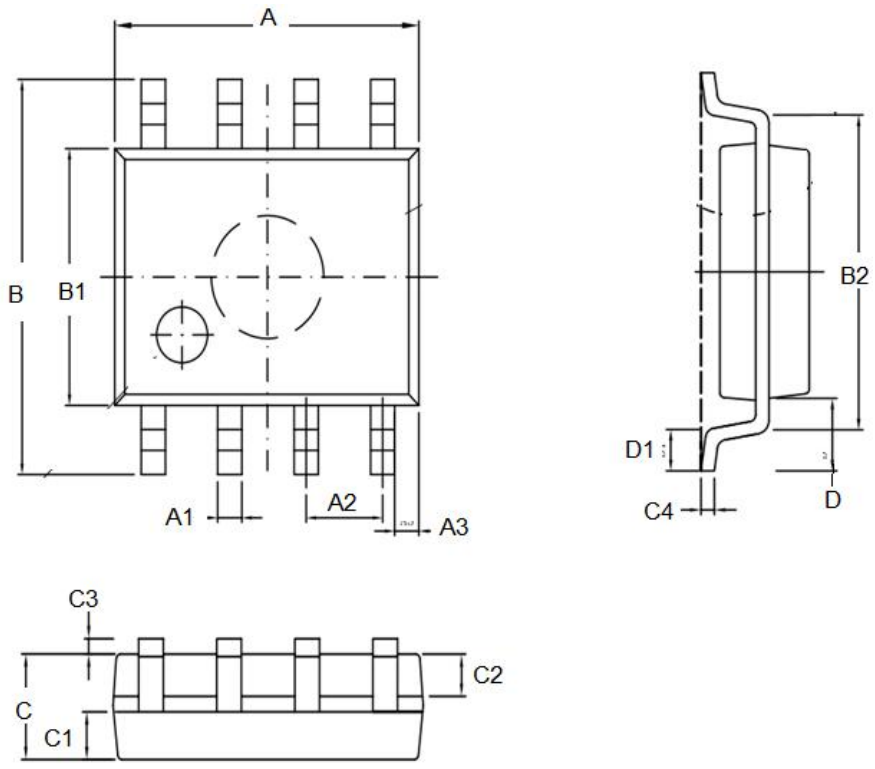
Ground Path: The GND path of the input power loop and IC controller path should be separated and connected at the negative terminal of input capacitor by single point, such as power sense resistor and the IC GND.

SOP-8 封装机械尺寸

SOP-8 MECHANICAL DATA

单位:毫米/UNIT：mm

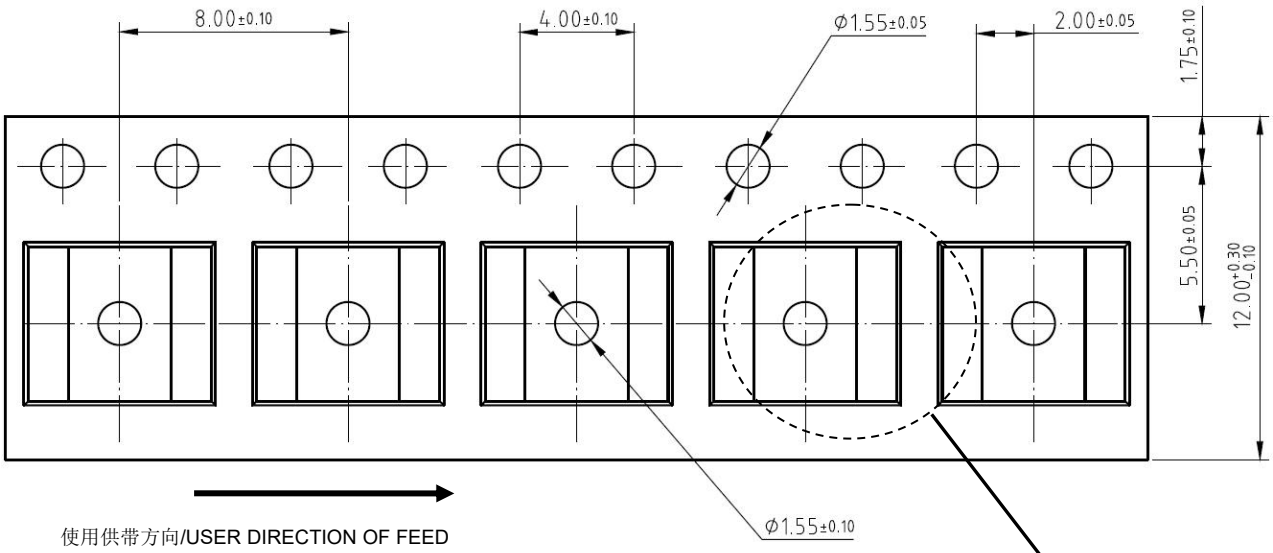
符号 SYMBOL	最小值 Min.	典型值 Typ.	最大值 Max.	符号 SYMBOL	最小值 Min.	典型值 Typ.	最大值 Max.
A	4.80		5.00	C	1.30		1.50
A1	0.37		0.47	C1	0.55		0.75
A2		1.27 TYP		C2	0.55		0.65
A3		0.41 TYP		C3	0.05		0.20
B	5.80		6.20	C4	0.19	0.20TYP	0.23
B1	3.80		4.00	D		1.05TYP	
B2		5.0TYP		D1	0.40		0.62

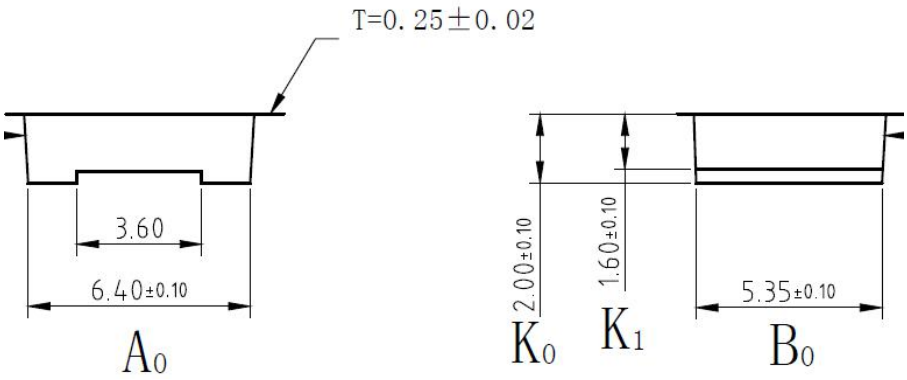


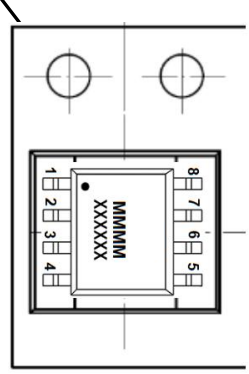
SOP-8 (13")编带规格

SOP-8 (13")TAPE AND REEL DATA

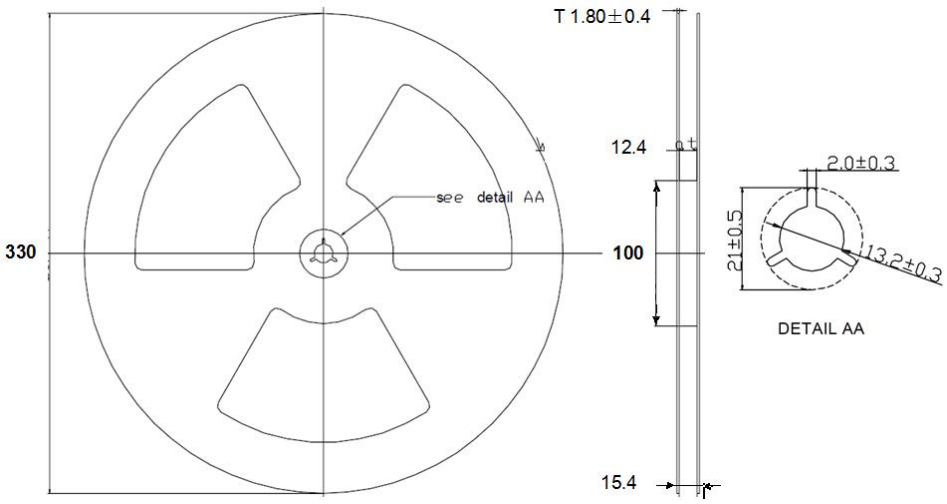
单位:毫米/UNIT：mm







器件定位示意图/UNIT ORIENTATION



13"卷盘/REEL

Revision history

Revision	Release data	Description
1.0	2019-06-02	Initial Version
1.1	2019-09-10	Update description